OPTIMIZING THERMAL RADIATOR DESIGNS USING THE VERITREK SOFTWARE

Lina L. Maricic and R. Scott Miskovish
ATA Engineering, Inc., San Diego, CA 92128

Jacob A. Moulton and Derek W. Hengeveld
LoadPath, Albuquerque, NM 87106

ABSTRACT

Thermal engineers at ATA Engineering, Inc., (ATA) wanted to utilize machine learning and reduced-order models (ROMs) to design the thermal radiators of a spacecraft, improving upon traditional thermal design and analysis techniques. A common problem exists in the aerospace industry when the thermal design is driven by minimizing survival power while maintaining compliance with allowable flight temperatures (AFTs) in a variable thermal environment. Finding an optimal design solution can be time-consuming and requires a large number of simulations. ATA used the Veritrek software to create a ROM to efficiently solve this complex problem and avoid an overdesigned thermal system.

A generic spacecraft model was created in Thermal Desktop® to emulate this problem. A six-sided box made of aluminum honeycomb sandwich panels, with electronics mounted on three side faces, was placed in a low Earth orbit (LEO). The constraints of the problem are twofold. First, the maximum temperatures of electronics in the worst-case hot (WCH) environment cannot surpass maximum AFTs of 40°C. Second, the duty cycle of survival powers used to maintain the electronics above the minimum AFTs cannot exceed 80% in the worst-case cold (WCC) environment. In order to determine the optimal radiator sizes given electronic power dissipations, ATA used Veritrek, a reduced-order thermal modeling software. Using Veritrek, ATA created a ROM to explore the thermal design space and find optimal radiator sizes. Two hundred fifty-six training data simulations were generated in the Veritrek Creation tool to create a reliable ROM, and the Veritrek Exploration Tool was used to identify and evaluate the optimized thermal system. In all, it took about five days to reach an optimal design solution using Veritrek, an effort that would have taken about one month using traditional thermal analysis techniques.

INTRODUCTION

Often in the aerospace industry, thermal engineers are faced with design problems that require management of thermal energy on both ends of the hot-cold spectrum. In the cold vacuum of space, heaters are a common design component to keep spacecraft electronics from getting too cold, while radiators are used to keep spacecraft electronics from getting too hot when the spacecraft is in direct sunlight and/or the internal electronics are running at full power. As a result, the challenge is minimizing survival power of the heaters while maintaining compliance within allowable flight temperature (AFT) ranges using radiators. Due to the high variability in thermal environment, along with many interrelated variable inputs that can be altered to try to satisfy this problem, finding an optimal design solution is complex and can be very time-consuming. Complexity makes thermal analysis difficult to execute, leading to a reduced

understanding of how the thermal system behaves. Traditional methods require numerous simulations using detailed thermal math models, but ATA Engineering, Inc., (ATA) wanted to find an alternative means to design thermal radiators of a spacecraft that utilized machine learning to create reduced-order models (ROMs). As a result, ATA used the Veritrek Creation Tool and Veritrek Exploration tool, to quickly reach an optimal design solution and better understand the thermal design. Making use of the Veritrek software allowed for more effective and efficient exploration of the spacecraft's thermal design in a shorter period of time.

Built for Thermal Desktop®, Veritrek (Figure 1) leverages the power of ROMs, which act as statistical emulators constructed from high-resolution simulations and enable thousands of simulations results in seconds. Since 2009, a robust method for creating accurate ROMs has been developed and tested for a wide range of applications, and has led to the development of the Veritrek Creation Tool. The Veritrek Creation Tool allows users to create ROMs from Thermal Desktop models. A user can then import the ROM into the Veritrek Exploration Tool to perform rapid thermal analysis in the form of 2-D and 3-D plotting, sensitivity studies, screening analyses, and optimization studies.

Figure 1. Veritrek software suite. Starting with a Thermal Desktop model, a user can create a ROM and use it to perform rapid thermal analysis using one of the five available analysis features.

ATA_SMALLSAT_BUS THERMAL MATH MODEL

To set up the problem and evaluate the approach, a thermal math model of a six-sided box made of aluminum honeycomb panels, representing a generic spacecraft, was created in Siemens NX11® and imported into Thermal Desktop (Figure 2) to solve. This ATA_SmallSat_Bus was 1.2 meters long, 1 meters wide, and 0.5 meters high, and had a total of five electronic boxes mounted on the inside of three faces.

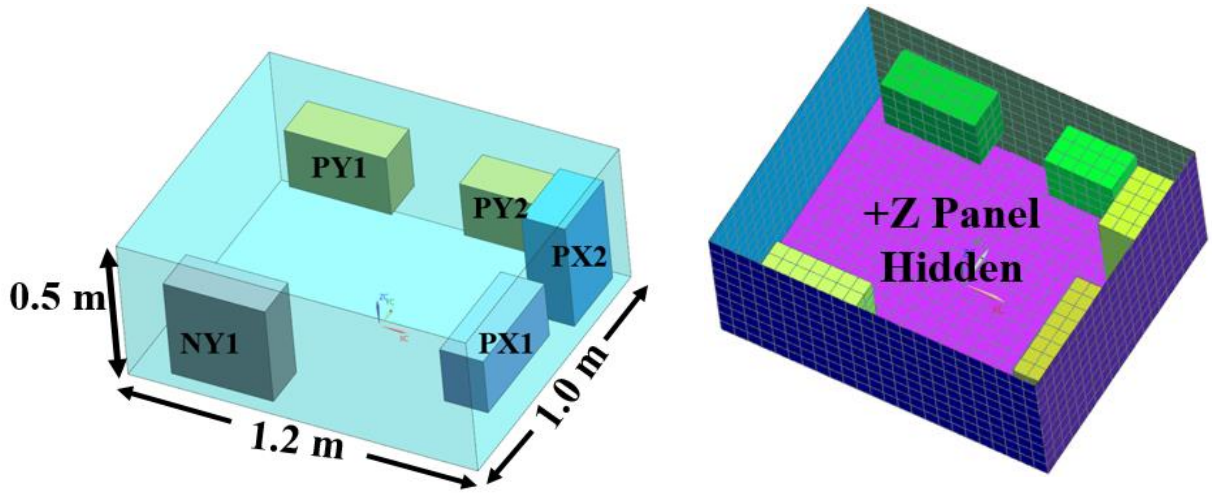


Figure 2. Thermal math model of the ATA_SmallSat_Bus.

This spacecraft orbits on a low Earth orbit (LEO) of the 1,000 km altitude. The orbit period is 6,298 seconds. In the worst-case hot (WCH) condition, the spacecraft orbits at a β angle of 60°, with its +Z axis pointing to the Nadir and its +X axis is the velocity direction (Figure 3). At this β angle, no eclipse occurs and the spacecraft has a full view to the Sun throughout the orbit. Electronics are in an operational mode and operating at their maximum powers. The summary of the electronics' maximum operational powers, along with the electronics nomenclature and placement, is shown in Table 1 and Figure 2. The electronics names are based on their location on the ATA_SmallSat_Bus, i.e., NY1 refers to the electronics on the negative Y face, PX1 refers to the first electronics on the positive X face, PX2 refers to the second electronics on the positive X face, PY1 refers to the first electronics on the positive Y face, and PY2 refers to the second electronics on the positive Y face. The same nomenclature is used for heaters and radiators names.

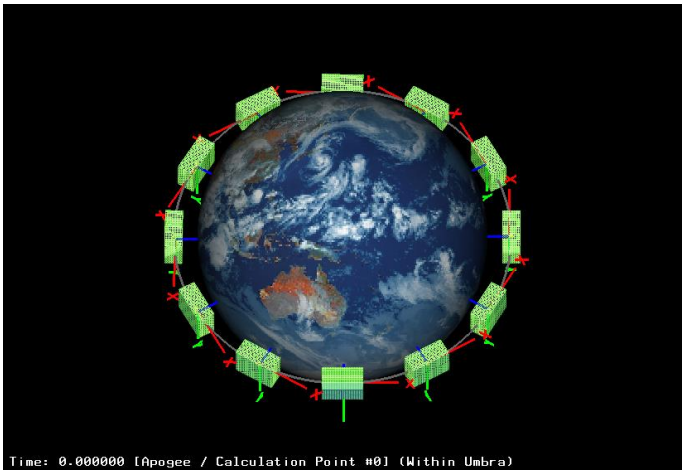


Figure 3. Spacecraft orbit and attitude in the WCH condition (view from the Sun).

Table 1. Summary of maximum operational powers of electronics in WCH condition.

Electronics	Maximum Operation Power (W)

PY1	60
PY2	30
NY1	30
PX1	50
PX2	30
Total	200

In the worst-case cold (WCC) condition, the spacecraft orbits at a β angle of 0°, with its −Z axis pointing to the Sun, and +Y axis pointing to the North (Figure 4). The electronics are not powered throughout the orbit. However, survival heaters are available and may be turned on to keep electronics above minimum AFTs.

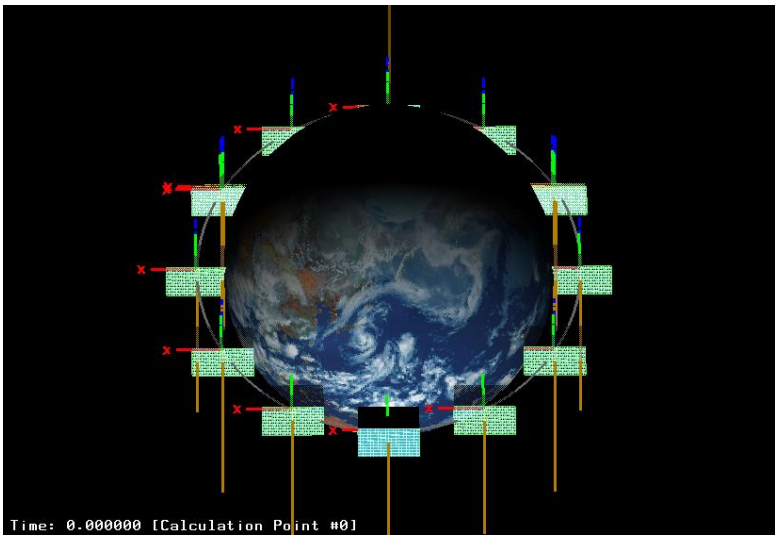


Figure 4. Spacecraft orbit and attitude in the WCC condition.

The constraints of the problem are twofold. First, the maximum electronics temperatures in the WCH environment cannot exceed maximum AFT of 40 °C. Second, the duty cycle of survival powers used to maintain the electronics above the minimum AFTs cannot exceed 80%. A summary of the five heaters' maximum powers and maximum allowable powers can be seen in Table 2. The heater names are based off of their location on the ATA_SmallSat_Bus, i.e., NY1 refers to the heater on the negative Y face, PX1 refers to the first heater on the positive X face, PX2 refers to the second heater on the positive X face, PY1 refers to the first heater on the positive Y face, and PY2 refers to the second heater on the positive Y face.

Table 2. Summary of survival powers and their design goal in WCC condition.

Heater Name and Side	Maximum Heater Power	80% of the Maximum Heater Power
NY1	55 W	44 W
PX1	80 W	64 W
PX2	20 W	16 W
PY1	55 W	44 W
PY2	40 W	32 W

Each electronics box has a dedicated radiator with a nominal or initial radiator area that is the same as the footprint of the electronic box (Figure 5). At the nominal condition, the full area of the −X face of the spacecraft is also a radiator. The rest of the spacecraft is covered with multilayer insulation (MLI) materials. The geometric center of each radiator is coincident with the center of the footprint of each electronics box on each spacecraft panel. The length of each radiator is a parameter and can be varied in the Thermal Desktop model. Each radiator's height-to-length ratio is the same as the electronics box footprint's height-to-length ratio. For the −X face radiator, the height-to-length ratio is the spacecraft −X face's height-to-length ratio. Therefore, the radiator area is determined by the length of each radiator. The range of each radiator's length was carefully selected so that the radiators are not overlapping with each other on the same face where two electronics are mounted, or their dimensions are not exceeding the length and height of the spacecraft faces on which they are attached.

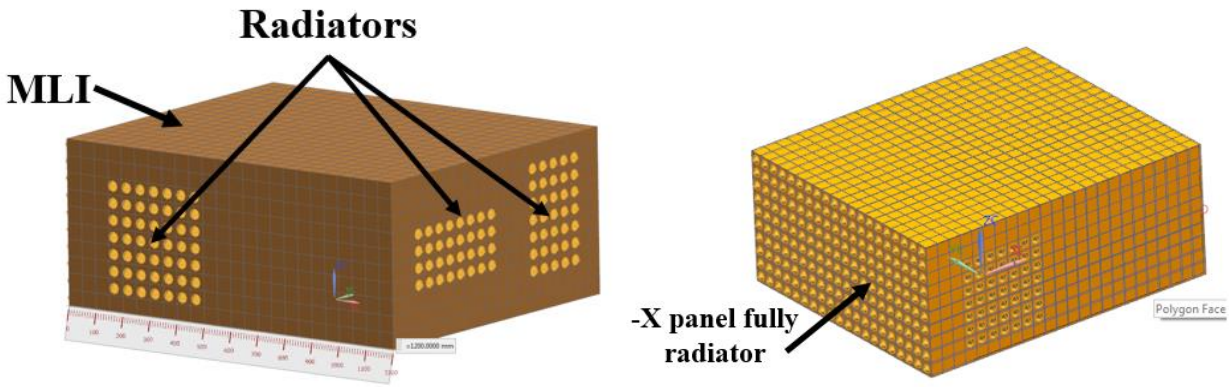


Figure 5. Nominal radiator sizes of the ATA_SmallSat_Bus.

REDUCED-ORDER MODEL DEVELOPMENT

ROMs are developed within the Veritrek Creation Tool using a statistical scheme based on sampling and data fitting an underlying Thermal Desktop model. This approach is considerably different from nodal reduction methods in that it relies on a set of high-fidelity simulation results (i.e., training data) to generate the ROM.

The first step in developing a ROM is carefully selecting sampling points. The Veritrek Creation Tool utilizes Latin hypercube sampling space-filling designs to efficiently identify and evaluate interior points that would provide improvements in the ROM. A Latin hypercube sampling algorithm was developed based on concepts of the maximin method [1].

Data fitting in the Veritrek Creation Tool is achieved using Gaussian process (GP) regression methods. Introduced for computer experiments by Sacks, Welch, Mitchell, and Wynn [2], this approach is desirable in computer experiments since it provides an exact fit to the training data and requires only k+1 parameters, where k is the number of input factors. GPs do not impose a specific model structure on the underlying function being modeled. Instead, a Gaussian prior is placed on the range of possible functions that could represent the mapping of input factors to output responses. The Gaussian prior incorporates knowledge into the data about the underlying function and is specified using the GP covariance function, which provides a relationship between training data points. Although several approaches can be utilized for this correlation structure, the approach used the squared exponential covariance function, one of the most common. As such, GP modeling is a nonparametric modeling technique, where the training data are used to discover the model properties in a supervised manner. Details of the implemented GP method can be found in prior work [1].

The ATA_SmallSat_Bus ROM was built to quickly determine optimal radiator sizes. The underlying Thermal Desktop model consists of multiple cases that include hot- and cold-case orbital environments, as well as symbols that change the size of six different body-mounted radiators. These six symbols were chosen as input factors for the ROM, along with the two case sets controlling the orbital environment. Ten output responses were selected; these include five electronics temperatures and five outputs that track the amount of heater power necessary to keep the spacecraft above its minimum AFT. These ROM parameters are outlined and described in Table 3 through Table 5.

Table 3. Summary of symbols used as input factors for the ATA_SmallSat_Bus ROM.

Symbol Name	Description
Radiator NX Lx	Size of the radiator on the –X face of the spacecraft. Ranges from 0.1 to 1.
Radiator NY Lx	Size of the radiator on the –Y face of the spacecraft. Ranges from 0.01 to 0.5.
Radiator1 PX Lx	Size of the first radiator on the +X face of the spacecraft. Ranges from 0.1 to 0.35.
Radiator1 PY Lx	Size of the first radiator on the +Y face of the spacecraft. Ranges from 0.1 to 0.6.
Radiator2 PX Lx	Size of the second radiator on the +X face of the spacecraft. Ranges from 0.1 to 0.5.
Radiator2 PY Lx	Size of the second radiator on the +Y face of the spacecraft. Ranges from 0.1 to 0.25.

Table 4. Summary of case sets used in the ATA_SmallSat_Bus ROM.

Case Set Name	Description
Cold Case	Sun –Z, North +Y, β = 0. Solar Flux = 1318 W/m^2. Earth IR Flux = 215. Albedo = 0.25.
Hot Case	Nadir +Z, Velocity +X, β = 60. Solar Flux = 1414 W/m^2. Earth IR Flux = 263. Albedo = 0.35.

Table 5. Summary of output responses used in the ATA_SmallSat_Bus ROM.

Output Response Name	Single Node	Node Group	Max Value
NY Elec Intfc Max Temperature (–Y Face)		X	X
PX Elec1 Intfc Max Temperature (+X Face)		X	X
PX Elec2 Intfc Max Temperature (+X Face)		X	X
PY Elec1 Intfc Max Temperature (+Y Face)		X	X
PY Elec2 Intfc Max Temperature (+Y Face)		X	X
Heater NY1.1 Max Power (–Y Face)	X		X
Heater PX1.1 Max Power (+X Face)	X		X
Heater PX2.1 Max Power (+X Face)	X		X
Heater PY1.1 Max Power (+Y Face)	X		X
Heater PY2.1 Max Power (+Y Face)	X		X

RESULTS AND DISCUSSION

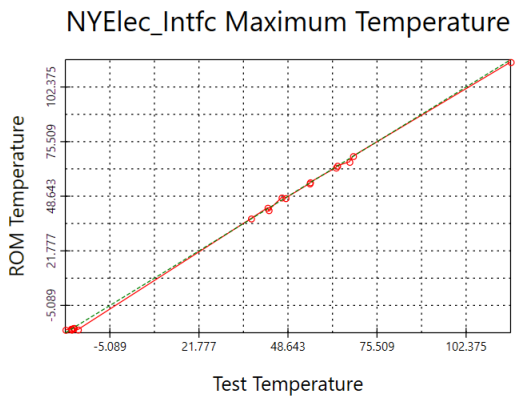
ATA_SmallSat_Bus ROM Results from the Veritrek Creation Tool

Three iterations of the ATA_SmallSat_Bus ROM were performed. Each iteration contained an increase in the number of training runs used to create the ROM, until the desired ROM accuracy metrics were realized. In addition to increasing the training data, LoadPath helped ATA better tune the ROM data fit by adjusting data fitting parameters available to the user. A summary of the number of sampling runs included in each iteration, along with the time it took to complete each iteration of the ROM are shown in Table 6. It is important to note that the time taken to create the ROM is continuous and automated, requiring little to no user intervention.

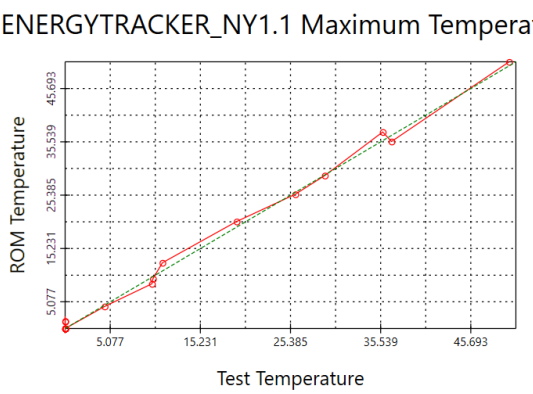
Table 6. Time taken to create the ATA_SmallSat_Bus ROM.

ROM Creation Iteration	# Training Runs	Time to Generate Training Data*	Time to Fit the Data	Time to Test the ROM	Total Time for ROM Creation
1	66	17 hours	1 hour	4 hours	~ 1.0 day
2	128	32 hours	2 hours	4 hours	~ 1.5 days
3	256	64 hours	16 hours	8 hours	~ 4.0 days
* The system used to generate the ROM was a Windows 10 laptop running AutoCAD 2018 and Thermal Desktop® 6.0 Patch 21. The processor on this system was a 4-core Intel Core i-7 at 2.80 GHz.					

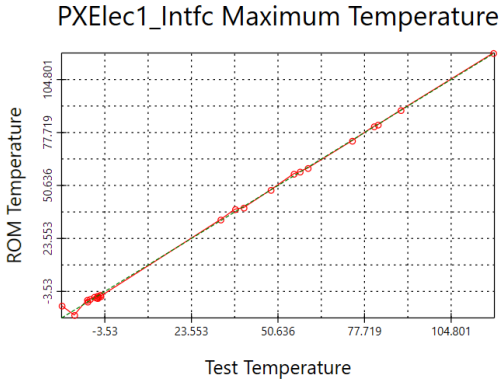
ROM performance was analyzed inside the Veritrek Creation Tool, using the ROM testing feature to directly compare how the ROM predictions perform relative to the underlying Thermal Desktop model. A user-defined number of test runs are performed in Thermal Desktop (note these runs are not the runs used for ROM creation), and then Veritrek uses the created ROM to predict the outputs for each of these runs. A comparison plot is generated for each output response. A green diagonal line is shown in the plot, which represents a perfect ROM prediction. The actual measured test points are shown as red dots. As shown in Figure 6, these red dots do not fall perfectly along this ideal line; and this is where the user makes the decision on whether the ROM is performing accurately enough for their intended application.


NYElec_Intfc Maximum Temperature
ROM Temperature
-5.089
21.777
48.643
75.509
102.375
Test Temperature

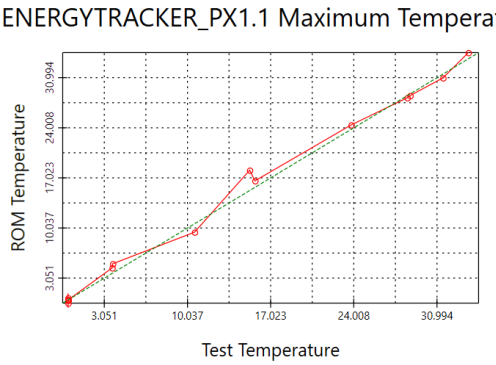
a.


ENERGYTRACKER_NY1.1 Maximum Temperature
ROM Temperature
5.077
15.231
25.385
35.539
45.693
Test Temperature

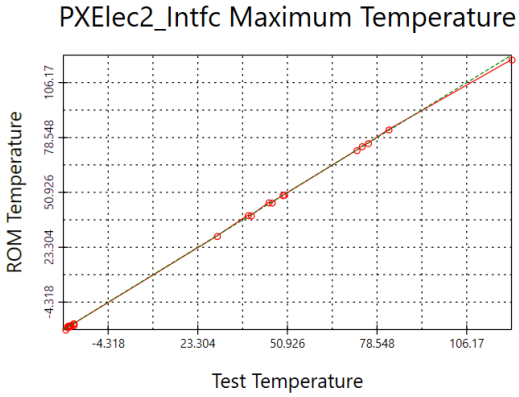
b.


PXElec1_Intfc Maximum Temperature
ROM Temperature
-3.53
23.553
50.636
77.719
104.801
Test Temperature

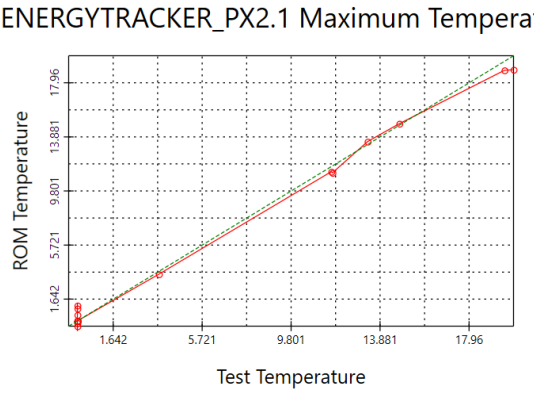
c.


ENERGYTRACKER_PX1.1 Maximum Temperature
ROM Temperature
3.051
10.037
17.023
24.008
30.994
Test Temperature

d.


PXElec2_Intfc Maximum Temperature
ROM Temperature
-4.318
23.304
50.926
78.548
106.17
Test Temperature

e.


ENERGYTRACKER_PX2.1 Maximum Temperature
ROM Temperature
1.642
5.721
9.801
13.881
17.96
Test Temperature

f.

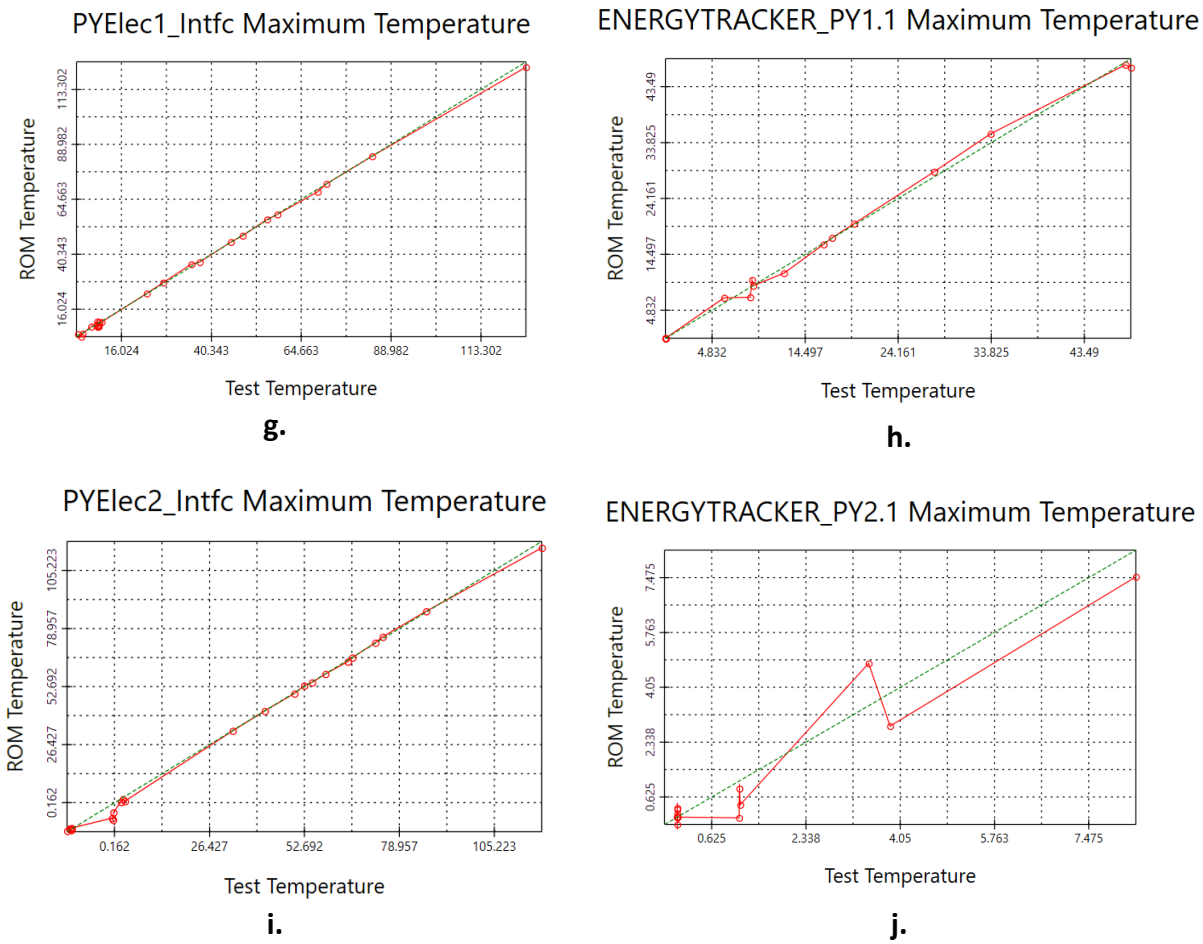


Figure 6. ROM versus Thermal Desktop performance comparison plots for the ten output responses, generated within Veritrek.

All data shown in these comparison plots was deemed acceptable by ATA. A few things to note are as follows:

1. In the current version of Veritrek, register values (such as the heater power used in this case study) are tracked using dummy boundary temperature nodes. As a result, for this ROM, there were five energy tracker nodes set up and used to store a register value. This is why the comparison plots show "ENERGYTRACKER_PY2.1 Maximum Temperature."

2. Figure 6f shows a cluster of test points that form a vertical line at a test temperature equal to 0. For the Thermal Desktop model, there will never be a heater power measured that is below 0, and so this hard discontinuous stop is more difficult for the ROM to handle. As a result, there were several test points where the heater was never turned on and so the test temperature is 0 but the ROM did not predict exactly 0 W of heater power.

3. The Thermal Desktop model induces a physical restriction that there cannot be negative power exhibited by the included heater, and so the lowest value is zero. The ROM just acts as a statistical emulator, and therefore cannot impose any physical

restrictions on a model. As a result, some results for the heater power output responses may be predicted as slightly negative by the ROM.

4. The plot for Figure 6j does not look as good compared to the other plots, but looking at the scale of the axes for the plot does relieve some of the initial concern. Overall, this output response only changes within about 9 W, regardless of the input factor settings. This is a good example of an output response with which the numerical residual data, discussed in the following paragraph, should be used in combination with the comparison plot to validate the accuracy of the ROM.

In addition to the comparison plots, the Veritrek Creation Tool also numerically calculates and measures ROM performance by way of the mean of the residual and standard deviation of the residual. These values are calculated from the difference between actual output results from Thermal Desktop, and results produced by the created ROM for each test run. These values should be used in combination with the comparison plots to determine whether the ROM is accurate enough. A summary of the residual mean and standard deviation for each of the ten output responses is shown in Table 7.

Table 7. Mean and standard deviation of the residual between ROM results and Thermal Desktop results as provided by the Veritrek Creation Tool.

Output Response Name	Mean of the Residual	Standard Deviation of the Residual
NY Elec Intfc Max Temperature (–Y Face)	−0.133 °C	0.764 °C
PX Elec1 Intfc Max Temperature (+X Face)	0.287 °C	1.496 °C
PX Elec2 Intfc Max Temperature (+X Face)	−0.019 °C	0.615 °C
PY Elec1 Intfc Max Temperature (+Y Face)	−0.197 °C	0.832 °C
PY Elec2 Intfc Max Temperature (+Y Face)	−0.928 °C	2.109 °C
Heater NY1.1 Max Power (–Y Face)	0.178 W	0.742 W
Heater PX1.1 Max Power (+X Face)	0.204 W	0.746 W
Heater PX2.1 Max Power (+X Face)	−0.021 W	0.443 W
Heater PY1.1 Max Power (+Y Face)	−0.007 W	0.710 W
Heater PY2.1 Max Power (+Y Face)	−0.094 W	0.476 W

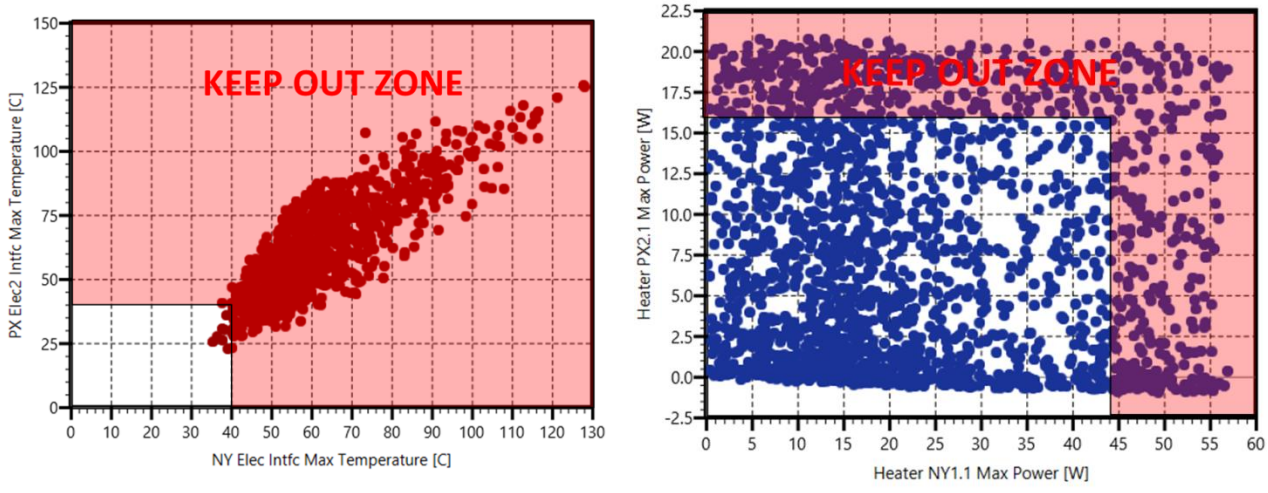
ATA's goal for the ATA_SmallSat_Bus ROM was output responses performing within 1 °C (or W) for the mean of the residual, and within 3 °C (or W) for the standard deviation of the residual. Table 7 results show that Veritrek was able to meet this goal for all ten output responses, using 256 sampling points to create the ROM. These results provided sufficient verification such that ATA engineers were confident to continue with using the ROM and the Veritrek Exploration Tool to obtain optimal radiator sizes for the ATA_SmallSat_Bus.

Optimal Radiator Size Results Obtained in the Veritrek Exploration Tool

The Veritrek Exploration Tool allowed for quick and efficient exploration of the thermal design space for the created ATA_SmallSat_Bus ROM. The Veritrek Exploration Tool includes five unique analysis features, which utilize a ROM to provide users with instant access to results and useful data plots. ROM data and results can also be exported into other software programs, such as Microsoft Excel or MATLAB, for any custom plotting. The five analysis features included with the Veritrek Exploration Tool include (1) Point Analysis, which acts as an Excel-like table; (2) Factor Sweep Analysis, which acts as a 2-D parametric sweep plotter; (3) Surface Plot Analysis, which performs two parametric sweeps at the same time to produce a 3-D response surface plot; (4) Screening Analysis, which uses statistical techniques to show the average effects input factors have on output responses; and (5) Optimization Analysis, which uses statistical techniques to show output response design envelopes for given values of input factors.

Using a combination of the Optimization Analysis and Point Analysis features, it was possible to quickly investigate all radiator size combinations and filter down to an optimal design solution for the ATA_SmallSat_Bus ROM. Optimization Analyses were used to filter out all input factor combinations that did not meet the output response criteria, and Point Analyses were used to check and further filter out runs by looking at all output response values at the same time.

During an Optimization Analysis, Veritrek randomly selects input factor values that are within a user-specified range and produces a single output response data point. Then, several thousands of these points can be generated very quickly to create a Pareto front plot that shows the design envelope for the designated output responses. Examples of the Optimization Analysis plots generated for this case study are shown in Figure 7.



a. **b.**

Figure 7. (a) Hot case maximum temperature and (b) cold case maximum power results from Veritrek's Optimization Analysis for two output responses.

For the hot cases, the ATA_SmallSat_Bus's heater does not turn on and so it is known that the heater power will be zero for all hot cases. As a result, only the maximum temperatures of electronics are the output responses of interest for hot cases (Figure 7a). For the cold cases, it is known that the maximum temperature will not approach the maximum AFT limit of 40 °C, and

so it is only the output responses tracking the maximum heater power necessary to keep the electronics above the minimum AFT that are of interest (Figure 7b).

Veritrek is able to generate these Optimization Analysis plots in a few seconds and provides access to tens of thousands of possible design solutions. Optimization Analysis plots similar to these were generated for all output response combinations, and these possible design solutions were filtered to those that fit within the output requirements for temperature and survival power. These filtered design solutions were imported back into Veritrek and a Point Analysis was used to make sure that they work for all output responses at the same time, which is essentially a second filtering step. After performing these steps, there were 35 point-design solutions acquired. Upon further evaluation of these 35 point-design solutions, and factoring in manufacturing feasibility and tolerances, it was deduced that these were all pointing toward a single optimal design solution. This preliminary optimal design solution is shown in the Point Analysis in Figure 8, and the practical design solution with tolerances is summarized in Table 8.

Orbits	Radiator NX Lx	Radiator NY Lx	Radiator1 PX Lx	Radiator1 PY Lx	Radiator2 PX Lx	Radiator2 PY Lx	NY Elec Intfc Max Temp... [C]	PX Elec1 Intfc Max Temp... [C]	PX Elec2 Intfc Max Temp... [C]	PY Elec1 Intfc Max Tem... [C]	PY Elec2 Intfc Max Temp... [C]	Heater NY1.1 Max Power [W]	Heater PX1.1 Max Power [W]	Heater PX2.1 Max Power [W]	Heater PY1.1 Max Power [W]	Heater PY2.1 Max Power [W]
Cold Case	0.95	0.32	0.33	0.435	0.41	0.25	-15.711	-8.460	-15.143	7.795	-1.675	32.410	32.663	12.078	39.276	2.820
Hot Case	0.95	0.32	0.33	0.435	0.41	0.25	39.584	31.446	31.614	32.247	35.748	0.000	0.000	0.000	0.000	0.000

Figure 8. Preliminary optimal design solution in Veritrek's Point Analysis.

Table 8. Preliminary optimal design solution.

Radiator Name	Optimal Size	Allowable Tolerance
Radiator NX Lx	0.950	± 0.050
Radiator NY Lx	0.320	± 0.060
Radiator1 PX Lx	0.330	± 0.020
Radiator1 PY Lx	0.435	± 0.025
Radiator2 PX Lx	0.410	± 0.030
Radiator2 PY Lx	0.250	± 0.005

The next step was to run this preliminary optimal design solution back in Thermal Desktop. Table 9 summarizes results from performing this single Thermal Desktop run, and all design requirements were met except for the PX2 Heater Power. The survival power duty cycle for this heater is shown as larger than 80% for this point design in Thermal Desktop.

Table 9. Preliminary optimal design results, Veritrek versus Thermal Desktop predictions.

Optimal Design	NY Elec Intfc Max Temp (−Y Face)	PX Elec1 Intfc Max Temp (+X Face)	PX Elec 2 Intfc Max Temp (+X Face)	PY Elec1 Intfc Max Temp (+Y Face)	PY Elec2 Intfc Max Temp (+Y Face)
Hot Case Veritrek Predict	39.3 °C	30.6 °C	28.4 °C	28.5 °C	33.8 °C
Hot Case TD Predict	36.8 °C	28.7 °C	27.9 °C	25.2 °C	33.0 °C
Difference	2.5 °C	1.9 °C	0.5 °C	3.3 °C	0.8 °C
Optimal Design	**Heater NY1.1 Max Power**	**Heater PX1.1 Max Power**	**Heater PX2.1 Max Power**	**Heater PY1.1 Max Power**	**Heater PY2.1 Max Power**
Cold Case Veritrek Predict	26.6 W	31.2 W	14.9 W	41.8 W	2.3 W
Cold Case TD Predict	26.3 W	23.1 W	19.6 W	35.9 W	9.7 W
Difference	0.3 W	8.1 W	−4.7 W	5.9 W	−7.4 W
Optimal Design	**Duty Cycle**				
Cold Case Veritrek Predict	48.4%	39.0%	74.5%	76.0%	5.8%
Cold Case TD Predict	47.8%	28.9%	97.8%	65.2%	24.4%
Difference	1%	10%	−23%	11%	-−19%

The results were not a major cause for concern, however, as it was recognized from the beginning that the ROM predictions will not be identical to those results produced from Thermal Desktop. Using the Veritrek Exploration Tool, ATA made slight adjustments in the preliminary optimal design solution within a few seconds to navigate to a final optimized design solution that Thermal Desktop predicted to meet all design requirements. Since the only output response not fitting in with requirements was the Heater PX2.1 Max Power, a Screening Analysis was performed using the Veritrek Exploration Tool to look at the sensitivity of this output response in terms of the input factor ranges determined by the ± tolerances shown in Table 8. An image of these results is shown in Figure 9.

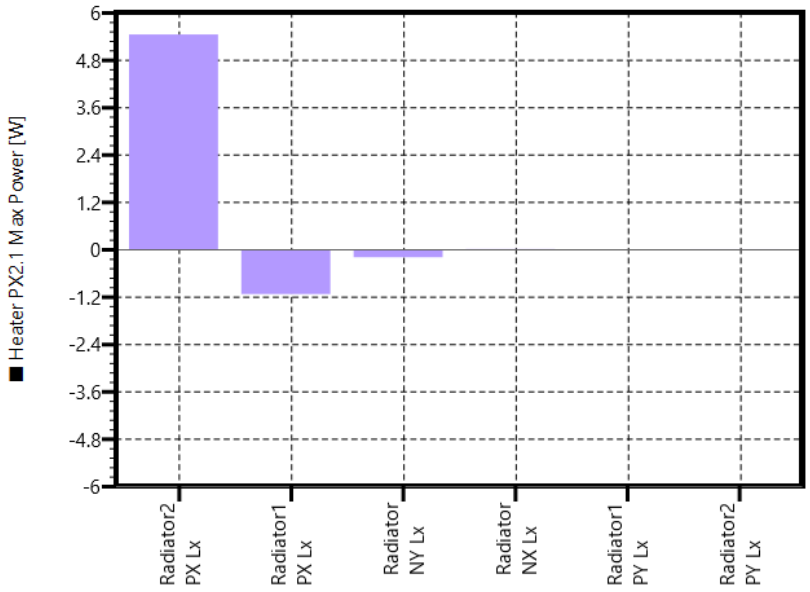


Figure 9. Sensitivity of Heater PX2.1 Max Power for preliminary optimal design solution.

The Screening Analysis shows the average effect that each input factor has on an output response. Each input factor's average impact is determined by taking its low value and all

combinations of the other input factor values, tracking the output response results and averaging those, and then doing the same thing for that input factor's high value and all combinations of the other input factor values. The difference between these two averages is then normalized to zero, and this process continues for all input factors. The result is bar graphs that show the average impact each input factor has on an output response.

These results show that reducing the size of Radiator2 PX Lx will reduce the Heater PX2.1 Max Power, as intuition would suggest. Using this info, ATA investigated a modified point design solution with the Point Analysis using the smallest Radiator 2 PX Lx size allowed by the tolerances shown in Table 8; this is 0.380. This modified point design solution ultimately became the final optimal design solution, shown in Figure 10 and Table 10.

Orbits	Radiator NX Lx	Radiator NY Lx	Radiator1 PX Lx	Radiator1 PY Lx	Radiator2 PX Lx	Radiator2 PY Lx	NY Elec Intfc Max Temp... [C]	PX Elec1 Intfc Max Temp... [C]	PX Elec2 Intfc Max Temp... [C]	PY Elec1 Intfc Max Temp... [C]	PY Elec2 Intfc Max Temp... [C]	Heater NY1.1 Max Power [W]	Heater PX1.1 Max Power [W]	Heater PX2.1 Max Power [W]	Heater PY1.1 Max Power [W]	Heater PY2.1 Max Power [W]
Cold Case	0.95	0.32	0.33	0.435	0.38	0.25	-15.709	-8.291	-15.189	7.868	-1.675	32.408	33.037	9.309	39.276	2.816
Hot Case	0.95	0.32	0.33	0.435	0.38	0.25	40.248	32.459	34.327	32.631	36.209	0.000	0.000	0.000	0.000	0.000

Figure 10. Final optimal design solution in Veritrek's Point Analysis.

Table 10. Final optimal design solution.

Radiator Name	Optimal Size	Allowable Tolerance
Radiator NX Lx	0.950	± 0.050
Radiator NY Lx	0.320	± 0.060
Radiator1 PX Lx	0.330	± 0.020
Radiator1 PY Lx	0.435	± 0.025
Radiator2 PX Lx	0.380	± 0.005
Radiator2 PY Lx	0.250	± 0.005

This modified point design solution was then run through Thermal Desktop, and all output response requirements were met as shown in Table 11.

Table 11. Final optimal design results, Veritrek versus Thermal Desktop Predictions.

Optimal Design	NY Elec Intfc Max Temp (−Y Face)	PX Elec1 Intfc Max Temp (+X Face)	PX Elec 2 Intfc Max Temp (+X Face)	PY Elec1 Intfc Max Temp (+Y Face)	PY Elec2 Intfc Max Temp (+Y Face)
Hot Case Veritrek Predict	40.2 °C	32.6 °C	34.3 °C	32.6 °C	36.2 °C
Hot Case TD Predict	38.1 °C	30.6 °C	33.1 °C	26.2 °C	34.4 °C
Difference	2.2 °C	2.0 °C	1.2 °C	6.4 °C	1.8 °C
Optimal Design	**Heater NY1.1 Max Power**	**Heater PX1.1 Max Power**	**Heater PX2.1 Max Power**	**Heater PY1.1 Max Power**	**Heater PY2.1 Max Power**
Cold Case Veritrek Predict	32.4 W	33.0 W	9.3 W	39.3 W	2.8 W
Cold Case TD Predict	26.4 W	23.9 W	14.7 W	35.9 W	9.8 W
Difference	6.0 W	9.1 W	−5.4 W	3.4 W	−7.0 W
Optimal Design	**Duty Cycle**				
Cold Case Veritrek Predict	58.9%	41.3%	46.5%	71.5%	7.0%
Cold Case TD Predict	48.0%	29.9%	73.5%	65.3%	24.5%
Difference	10.9%	11.4%	−27%	6.2%	−17.5%

FUTURE WORK

ATA would like to apply this technique in a real-life example where radiator designs are more realistic and complex. It may involve more design constraints and design variables, and thus more computation time and power.

The Veritrek Creation and Exploration Tools were used to identify an optimized thermal design solution in 85% less time that it would have taken using traditional methods. However, there are still several enhancements, based on user feedback, planned for future releases. For example, this work identified optimization analysis improvements that can be made to streamline the filtering process within Veritrek. An improvement like this would allow users to save even more time, compared to using traditional thermal design and analysis techniques, in use cases similar to this one.

CONCLUSIONS

In conclusion, the Veritrek software proved very valuable in optimizing thermal radiator designs. Specifically, the Optimization Analysis was a very effective tool to use for this type of design problem, as it provided access to tens of thousands of possible design solutions and assisted in the filtering though this data to narrow down to an optimized design solution. The ATA_SmallSat_Bus ROM was created and tested to prove its validity and accuracy relative to the underlying high-fidelity Thermal Desktop model, and all of this was conducted in a semi-automated fashion with the Veritrek Creation Tool in approximately four days. After that, an optimized design solution was discovered within the Veritrek Exploration Tool in a matter of minutes. As a result, this optimized design solution was obtained in about five days from start to finish—an effort that would likely have taken about a month to complete using traditional thermal analysis techniques and approaches. This resulted in time savings close to 85%. In addition to the time savings, Veritrek provided much more insight into the thermal analysis data than could typically be achieved with traditional methods. This ultimately leads to less uncertainty, more confidence in a thermal design, and a more optimized thermal system.

CONTACT

Lina Maricic | Senior Project Engineer | ATA Engineering |13290 Evening Creek Drive South, San Diego, CA 92128 | lina.maricic@ata-e.com | (858) 480-2051

R. Scott Miskovish | Technical Director, Thermal | ATA Engineering |1500 Perimeter Parkway Suite 285, Huntsville, AL 35806 | scott.miskovish@ata-e.com | (256) 258-8409

Jacob Moulton | Staff Engineer | LoadPath, LLC | 3333 South Bannock St., Ste. 850 | Englewood, CO 80110 | jmoulton@loadpath.com | 505.401.4853 | www.loadpath.com

Derek Hengeveld, PhD, PE | Senior Engineer | LoadPath, LLC | 2309 Renard Place SE, Ste. 101 | Albuquerque, NM 87106 | dhengeveld@loadpath.com | 605.690.1612 | www.loadpath.com

NOMENCLATURE, ACRONYMS, ABBREVIATIONS

k	number of input factors
AFT	allowable flight temperatures
GP	Gaussian process
LEO	low Earth orbit
ROM	reduced-order model
WCC	worst-case cold
WCH	worst-case hot

REFERENCES

1. Hengeveld, D. W., & Biskner, A. (2017). Enhanced data exploration through Reduced-Order Models. *47th International Conference on Environmental Systems.* Charleston, SC

2. Sacks, J. W. (1989). Design and analysis of computer experiments. *Statistical science*, 409-423.

3. Tyler M. Schmidt, S. C. (2018). Thermal Design of a Mars Helicopter Technology Demonstration Concept. *ICES 2018.* Albuquerque.