Veritrek Creation Tool
User's Manual

Veritrek 4.0

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PREPARED, DISTRIBUTED, AND SUPPORTED BY

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REVISION HISTORY

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Veritrek Creation Tool	Veritrek 2.2 beta	May 2018
Veritrek – Creation Tool	Veritrek 2.2	August 2018
Veritrek – Creation Tool	Veritrek 2.2.1	September 2018
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Veritrek – Creation Tool	Veritrek 3.2.3	December 2020
Veritrek – Creation Tool	Veritrek 4.0.0	January 2021

SYSTEM REQUIREMENTS

Veritrek supports Windows 10 (64-bit only) operating systems.

The *Veritrek Creation Tool* requires the following:

- Autodesk's AutoCAD® (2016, 2017, or 2018)
- Cullimore and Ring Technologies' Thermal Desktop® (6.0.14 or newer including 6.1) and SINDA/FLUINT products including their required dependencies (e.g., Intel Fortran Compiler, etc.)
- Anaconda3 version up to 5.2.0
- Python version up to 3.6.5
- Python GPy version 1.9.6 and associated python packages (numpy, scipy, six, decorator, paramz)

Please refer to the *Veritrek 4.0 Installation Instructions Manual* for more information on system requirements.

Veritrek 4.0.0 - Creation Tool

New Features:

Divide and Merge – This feature has been added to the **ROM Setup & Summary** tab, and allows for a user to divide an .lpxml file into multiple .lpxml files or merge multiple .lpxml files into a single .lpxml file. This will allow for parallelizing ROM creation, merging multiple training data sets, and importing already-created test data. See Section 3.5.5 for more details.

ROM Parallelization – This feature has been added, allowing users to open up an .lpxml file in a "Parallel Only" mode, as opposed to the traditional "Full Feature" mode, that limits capability to just generating training data. If a user has multiple Thermal Desktop® licenses to use, this feature can be utilized to generate training data in parallel on the same machine or across multiple machines.

General:

A temporary folder system has been added to the ROM creation step. User's will notice a temporary folder get created adjacent to their .lpxml file which stores the .dwg file and associated files that *Veritrek* uses during ROM creation. As a result, users must now add .rco and .tdp property overwrites to their underlying Thermal Desktop® model. See Section 2.3 for more details.

Capabilities have been added to the *Veritrek Creation Tool* save structure, making it easier to move a model and .lpxml file to a new location.

The naming convention of output responses has been altered, such that the most pertinent information shows up first.

A check on the Initial conditions' files for the underlying Thermal Desktop® model has been added to Model Checks.

A note has been added to the **ROM Summary** tab to make users aware that once a ROM is created and imported into the *Veritrek Exploration Tool*, any changes made to the ROM in the *Veritrek Creation Tool* will not automatically move to the *Veritrek Exploration Tool*. A user must re-import an updated ROM into the *Veritrek Exploration Tool* to see any ROM changes.

Several bug fixes have been implemented, and are summarized below:

- A memory leak bug with the data-fitting step has been corrected.
- An issue with automatically saving the .lpxml after the data fit is complete has been corrected.
- "Estimated Time Left" tracker has been improved.

Menu and Toolbars:
No new menus or toolbars have been added at this time.

Veritrek 3.2.2 - Creation Tool

New Features:
No new features have been added at this time.

General:
A compatibility issue with the latest scipy package version issue was corrected.

Menu and Toolbars:
No new menus or toolbars have been added at this time.

Veritrek 3.2.1 - Creation Tool

New Features:
No new features have been added at this time.

General:
A compatibility issue with the latest Thermal Desktop® and SINDA patches was corrected.

Menu and Toolbars:
No new menus or toolbars have been added at this time.

Veritrek 3.2.0 - Creation Tool

New Features:
The **Optional ROM Improvement** tab has been added as a new feature. This allows a user to add more training runs to an already-existing ROM. If the first attempt at creating a ROM does not perform accurate enough, a user can use this feature to build on top of their already-created ROM instead of having to start from the beginning of the ROM creation process. This feature is detailed in Section 3.8.

General:
Several bug fixes have been implemented, and are summarized below:

- Functionality of the *Import Test Runs* button on the **ROM Testing** tab has been fixed.
- A check has been added to the *Check Inputs* functionality, that will not allow a user to proceed with their ROM creation without the selection of at least one continuous input factor.
- The saving, unlocking, and automatic transition to the next tab has been made more consistent.
- The *Open Help* button functionality has been fixed in the "Missing Software" window.
- Values for the training runs and test runs cannot be edited in the Creation Tool GUI tables.
- *Veritrek*'s checks on the Thermal Desktop® model now include whether a register is getting exported to SINDA.
- The Activity Log and Data Tracker now get updated during File>Open.

Menu and Toolbars:
Restore Default Settings has been added as an option in the Help Menu.

Veritrek 3.1.0 - Creation Tool

New Features:
No new features have been added at this time.

General:
Veritrek is now compatible with Thermal Desktop® version 6.1.

Menu and Toolbars:
No new menus or toolbars have been added at this time.

Veritrek 3.0.0 - Creation Tool

New Features:
Registers have been added as an output response option for users to select in the **Outputs** tab.
Incident Heat has been added as an output response option for users to select in the **Outputs** tab.
Insulation Nodes have been added as an output response option for users to select in the **Outputs** tab.

General:
Several bug fixes have been implemented, and are summarized below:

- Default value behavior for the # Training Runs/Category and # Validation Runs/Category have been fixed so that they will always show the current number of training runs the user has included in their ROM generation.
- The "Save As" operation has been fixed such that a user can save their ROM.lpxml file with a new name, without having to delete the ROM's data-fit.
- ROM naming improvements have been made such that some special characters that caused issues with saving locations can no longer be used.
- The "Import Test Runs" button has been fixed so that users can import unique test runs if desired.

Menu and Toolbars:
No new menus or toolbars have been added at this time.

Veritrek 2.2.2 - Creation Tool

New Features:
No new features have been added at this time.

General:
Improvements have been made to the data-fitting algorithm used during ROM creation. These improvements should result in more accurate ROMs.

Menu and Toolbars:
No new menus or toolbars have been added at this time.

Veritrek 2.2.1 - Creation Tool

New Features:
No new features have been added at this time.

General:
Workflow functionality has been improved by adjusting the color of some of the buttons throughout the Veritrek Creation Tool, to add more consistency and establish a general button color code. All buttons that are part of the main workflow (i.e. that a user will have to click in order to proceed with proper use of the tool) are colored **GREEN**; buttons that will pause or stop automatic workflow in progress are colored **RED**, and other buttons that present different options to the user outside of the main workflow are colored **BLUE**.

Menu and Toolbars:
No new menus or toolbars have been added at this time.

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1 OVERVIEW

Developed to enhance the capabilities of Cullimore and Ring Technologies' (CRTech) Thermal Desktop® (TD), *Veritrek* produces thousands of simulation results in seconds by leveraging the power of reduced-order models (ROMs). ROMs act as statistical emulators built from high-fidelity simulations and allow you to quickly investigate variations in your Thermal Desktop® model. Veritrek benefits include reduced modeling costs and accelerated analysis schedules using ROMs, more optimized designs through unique statistically based analysis features, and a more collaborative work environment through *Veritrek*'s easy-to-use interface and flexible licensing approach. Figure 1-1 shows a flowchart for the overall *Veritrek* process, including both the *Veritrek Creation Tool* and *Veritrek Exploration Tool*, along with the interaction between *Veritrek* and Thermal Desktop®.

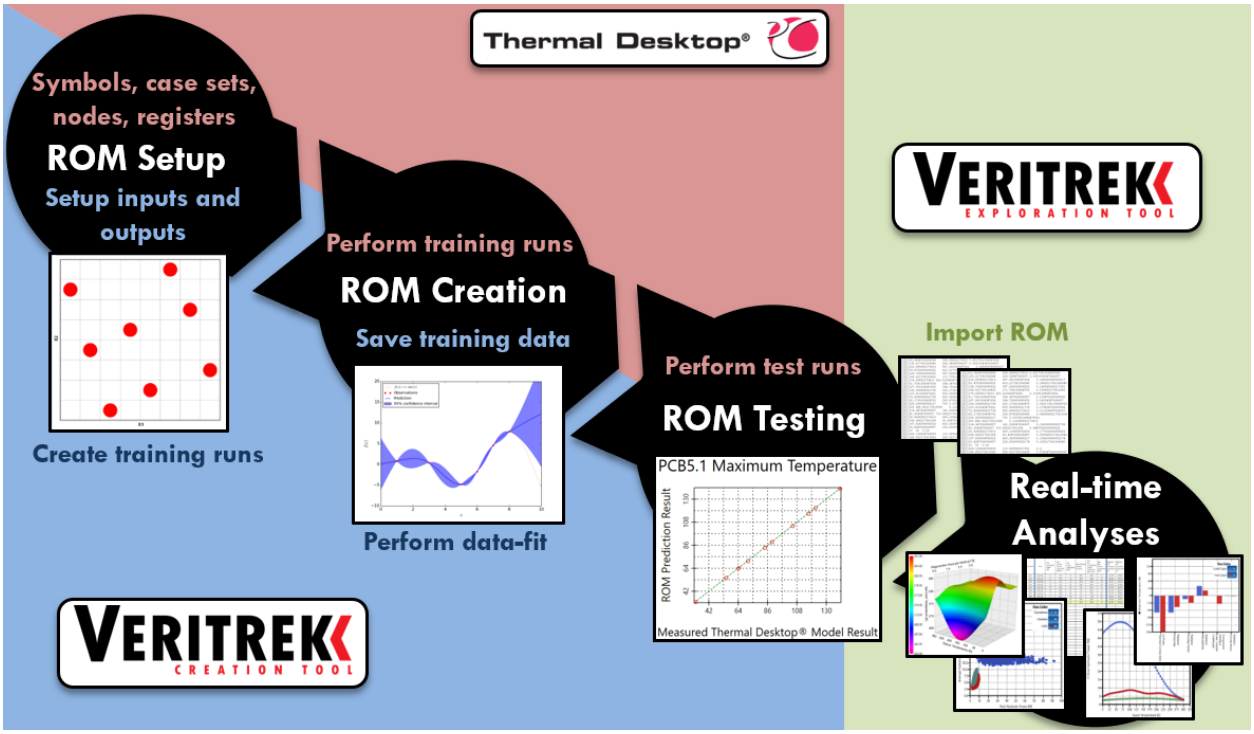


Figure 1-1: *Veritrek* process flowchart

This reference document is intended as a guide for a user of the *Veritrek Creation Tool*, as well as an explanation of how the tool works in the different features that it provides. The *Veritrek Creation Tool* allows a user to create a ROM from a Thermal Desktop® model, in a semi-automated fashion. The *Veritrek Creation Tool* creates a duplicate copy of a user's Thermal Desktop® model, stores it in a temporary folder, and uses this duplicate copy to perform all the necessary Thermal Desktop® runs and model manipulation. After the ROM creation process is complete, this duplicate copy is removed and in this way the user's original Thermal Desktop® model remains untouched.

This manual is intended for first-time users who need more detailed information on how the application tool works. Tutorials are shown with step-by-step instructions in Section 4, and more information on *Veritrek* can be found at http://veritrek.com/.

1.1 Overview of the *Veritrek Creation Tool*

The *Veritrek Creation Tool* was created to bridge the gap between detailed and reduced-order thermal models to meet the need of evaluating different thermal control subsystem (TCS) approaches and thermal design tradeoffs. The *Veritrek Creation Tool* is a tool that generates a reduced-order model (ROM) that represents a high-fidelity Thermal Desktop® (TD) model. It creates the ROM by varying user-specified input parameters for the selected case sets in TD, fitting the TD data to the outputs requested from the TD models, and then validating the data-fit by comparing different combinations of inputs to the original TD model. The result is a set of files that contain the ROM details and fitting coefficients used to define the ROM. The ROM can then be easily imported into the *Veritrek Exploration Tool*; to obtain thermal analysis results in near real-time.

The *Veritrek Creation Tool* graphical user interface (GUI) steps the user through the ROM creation process in an intuitive process flow and features automated interaction with Thermal Desktop®. The first step is titled **Model Selection**, in which a TD file to be converted into a ROM is selected and given a name. The second step is titled **Inputs**, and this is where input factors to be controlled in the ROM are selected from a list of Thermal Desktop® symbols. The **Outputs** tab is the third step, and this is where output responses to be created in the ROM are selected from individual nodes or entire node groups from TD submodels. These output responses resemble the variables of interest during the thermal analysis. The fourth step is called **ROM Setup & Summary**, and this is where the ROM to be created is set-up by selecting sampling and data-fitting schemes and their corresponding parameters. The fifth step is called **ROM Creation Status**. This is the step where the ROM gets created by communicating with Thermal Desktop® and running several Thermal Desktop® runs. The ROM is tested in the sixth step titled **ROM Testing**, and results are generated to show how closely the ROM compares to the under-lying TD model for a random set of runs. If testing results show that the ROM is not accurate enough for its intended rapid thermal analysis purpose, the **Optional ROM Improvement** tab is an optional seventh step that allows a user to add more sampling points to an already-existing ROM. Keep in mind that adding more sampling points will likely result in improved ROM accuracy but comes with the trade of performing more Thermal Desktop® training runs. After these seven steps, the ROM is complete, and a summary of the ROM can be seen in the **ROM Summary** tab.

1.2 Current V*eritrek* Capabilities and Limitations

The following provides information on the current capabilities that *Veritrek* offers, as well as some insight into future capabilities that are planned to become available for the *Veritrek Creation Tool*. Solutions to frequently encountered issues can be found in Section 2.3; however, this section provides high level information on the current capabilities and limitations of the *Veritrek* software. This list has been determined by user feature requests. These feature requests will help guide future development efforts and represent general limitations and current capabilities of the software.

- Allow for specific categorical input factor values, i.e., adding the ability to select specific values for categorical input factors other than the Integer and MinMax interpolation types.
- Include option to save complete data sets for each TD run that is performed during ROM creation.
- Include convergence criteria throughout the ROM creation to avoid unnecessarily performing more sampling runs.
- Provide the ability to evaluate inputs with uncertainty/probability distributions.
- Allow ROMs to be created from TD models that save results as .csr folders, rather than just .sav files.
- Add ability to select a window of time in a transient orbit to track output responses.

2 THERMAL DESKTOP® MODEL REQUIREMENTS

This documentation assumes familiarity with AutoCAD and Thermal Desktop®, and as such deals only with TD items specifically required for the *Veritrek Creation Tool*. For more information on these programs, please consult their respective user's manuals or help files.

The *Veritrek Creation Tool* imposes few and easy-to-satisfy, but important, requirements on the starting high-fidelity TD model. Section 2.1 defines the TD entities required by the *Veritrek Creation Tool*, Section 2.2 discusses how to properly use multiple case sets for ease of application tool use, and Section 2.3 provides a brief summary of the important settings that a TD model must have in order to successfully work with the *Veritrek Creation Tool* along with items that have presented themselves as the most common hang-ups for users. Section 2.3 can be thought of as a summary of solutions to frequently encountered issues.

2.1 Required Thermal Desktop® Entities

Three TD entities are required: nodes, symbols, and case sets.

Nodal characteristics (i.e., temperature) are used as output responses in the *Veritrek Creation Tool*. Nodes in submodels that are not built by all input case sets cannot be used as outputs.

Symbols can be used by TD to define virtually any value in a TD model as a variable. Symbols are used to define the input factors that will vary in the creation of the ROM. Symbols can be real or integer values. Symbols that are defined by other symbols or expressions cannot be used as input factors to the *Veritrek Creation Tool*; and symbols defined as arrays or strings cannot be used as inputs to the *Veritrek Creation Tool* either, as they are currently ignored by the *Veritrek Creation Tool*.
*** Helpful Tip – If there is a symbol defined by an expression that is desired to be used as an input factor, simply change its value to something discrete in the TD model so that it can be imported and used by the Veritrek Creation Tool.*

Case sets are used to define different orientations or other conditions that cannot be varied using a symbol. For example, case sets can be used to define different orbits or environmental parameters. Case sets cannot override symbols selected as input factors to the *Veritrek Creation Tool*. Case sets must save results to a *.sav* file, see Section 2.3 for more details. Case set results must include temperature results for all nodes selected as outputs in the *Veritrek Creation Tool*.

2.2 Conditions that Require Multiple Case Sets

For most conditions, a single TD case set can be used by the *Veritrek Creation Tool* since symbols can be used to alter nearly all the values used by a case set. However, there are some parameters that cannot be changed by symbols. These parameters are typically selected by radio buttons, checkboxes, or pull-down menus within TD. This section documents some of these conditions; however, there may be other conditions that require multiple case sets that are not shown.

2.2.1 Orbit Parameters

There are many options for orbital definitions within TD (Figure 2-1). To include different orbit types as inputs to the *Veritrek Creation Tool*, each of the orbit types will require its own case set. Likewise, there are several pointing options (Figure 2-2) and an orientation override option (Figure 2-2) to define the orbit that will require a unique case set for each option. Also, if various planetary orbits (Figure 2-3) or the spin of the satellite need to be altered to create the ROM, a new case set will be needed for each option.

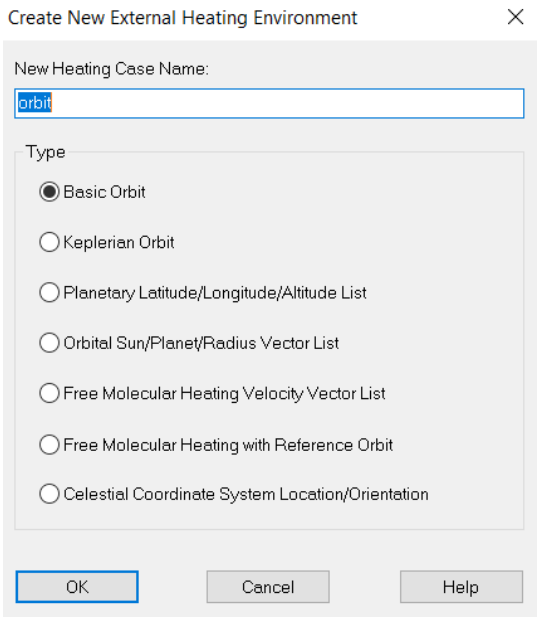


Figure 2-1: Multiple case-sets for orbit-type

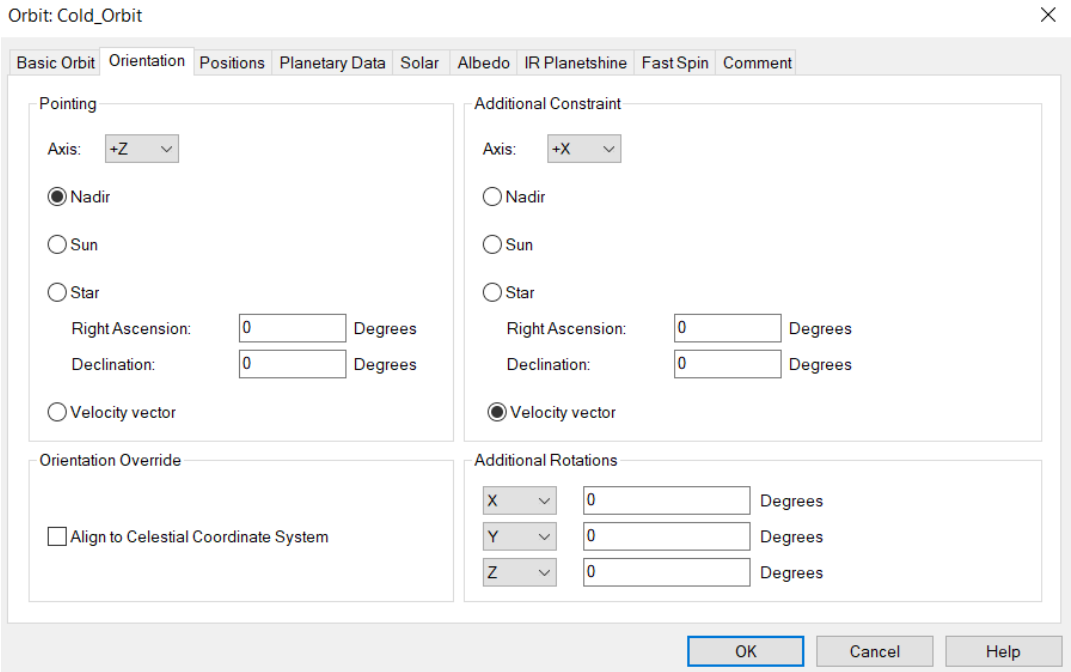


Figure 2-2: Multiple case-sets for varying pointing or orientation

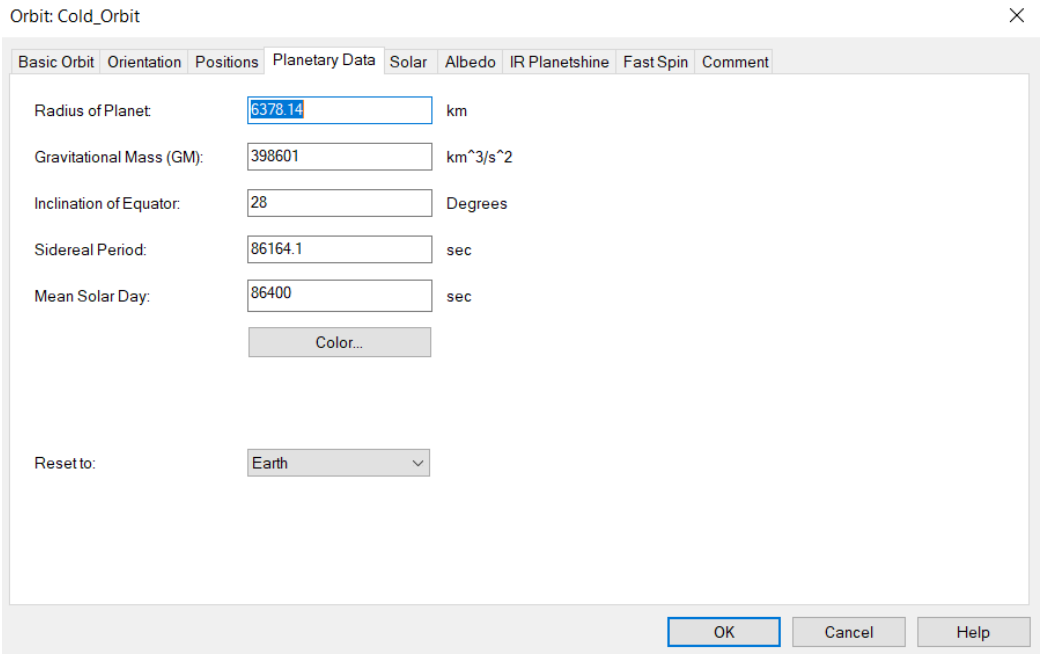


Figure 2-3: Multiple case-sets for different planetary orbits

2.2.2 Non-orbit Case Set Parameters

If the solution type (Figure 2-4), SINDA options (Figure 2-5), or symbol overrides (Figure 2-6) are to be included as input factors in the *Veritrek Creation Tool*, each set of options will need its own case set.

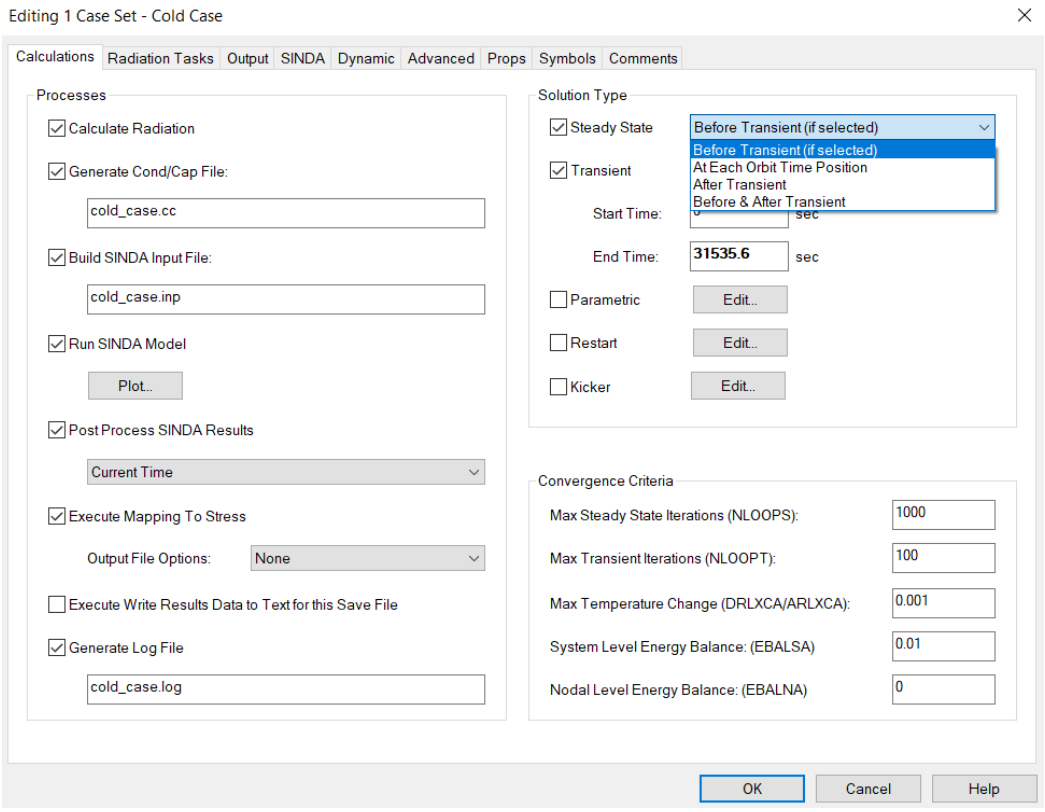


Figure 2-4: Multiple case-sets to use a solution type

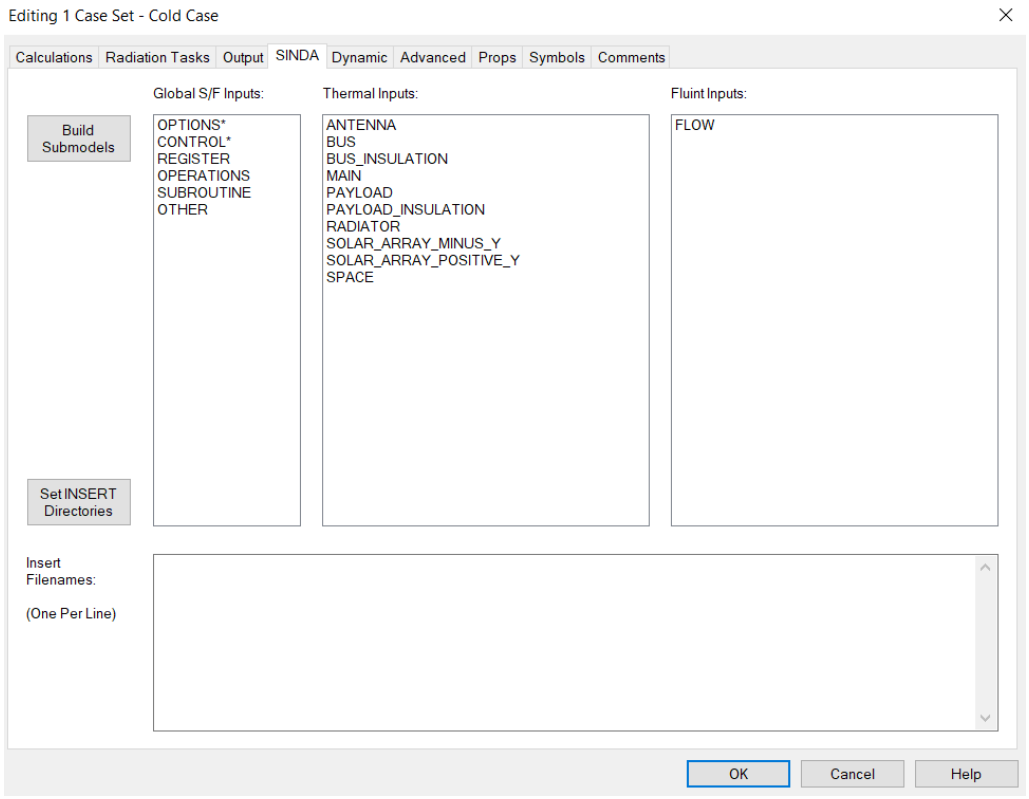


Figure 2-5: Multiple case-sets for varying SINDA options

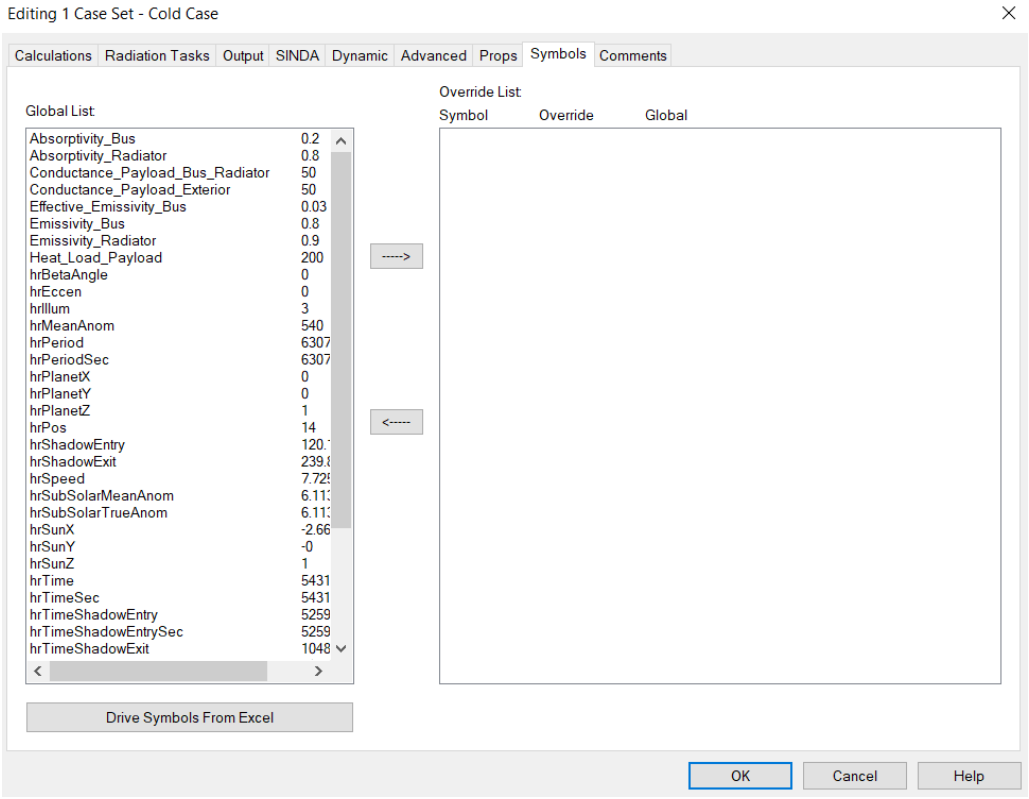


Figure 2-6: Multiple case-sets for symbol override

2.3 Summary of TD Model Requirements and Settings

The following information represents some helpful tips in setting up the underlying TD model for successful *Veritrek* use. These tips have come from interaction with users and can be looked at as solutions to frequently encountered issues regarding the necessary TD model settings.

Symbols, nodes, and case sets are required: See Section 2.1 for more details.

***Veritrek* cannot use a symbol whose value is an expression:** To use a symbol as an input factor, *Veritrek* currently requires that the symbol must be set up with a value inside of TD and not an expression that utilizes a formula or another symbol's value. As the TD symbols are imported into *Veritrek*, this pop-up will appear that describes the symbols that were skipped during the import process because they utilize expressions.

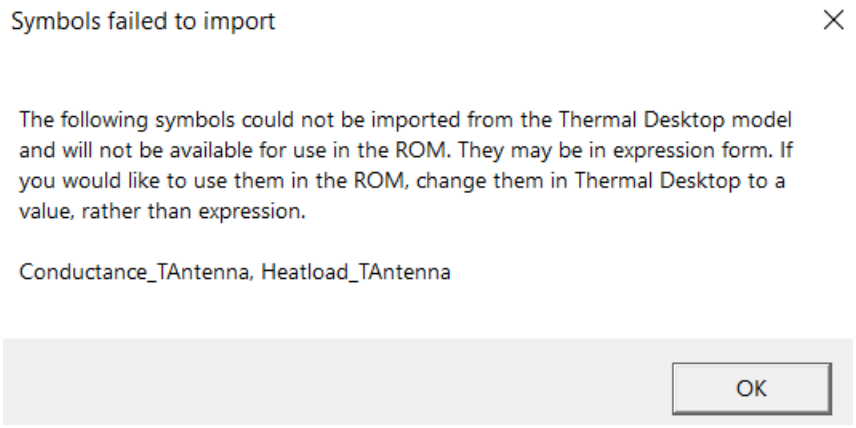


Figure 2-7: Skipped symbols pop-up for symbols that use expressions

To remedy this issue, simply go into the TD model and set the symbols value to a discrete value rather than an expression. The symbol can then be imported into *Veritrek* and used as an input factor for the ROM.

Case sets must include the RUN SINDA option: *Veritrek* currently requires the RUN SINDA option to be selected for each case set to be utilized in the ROM. This setting can be found in the Calculations tab when editing a Case Set from the Case Set Manager and is shown in Figure 2-8.

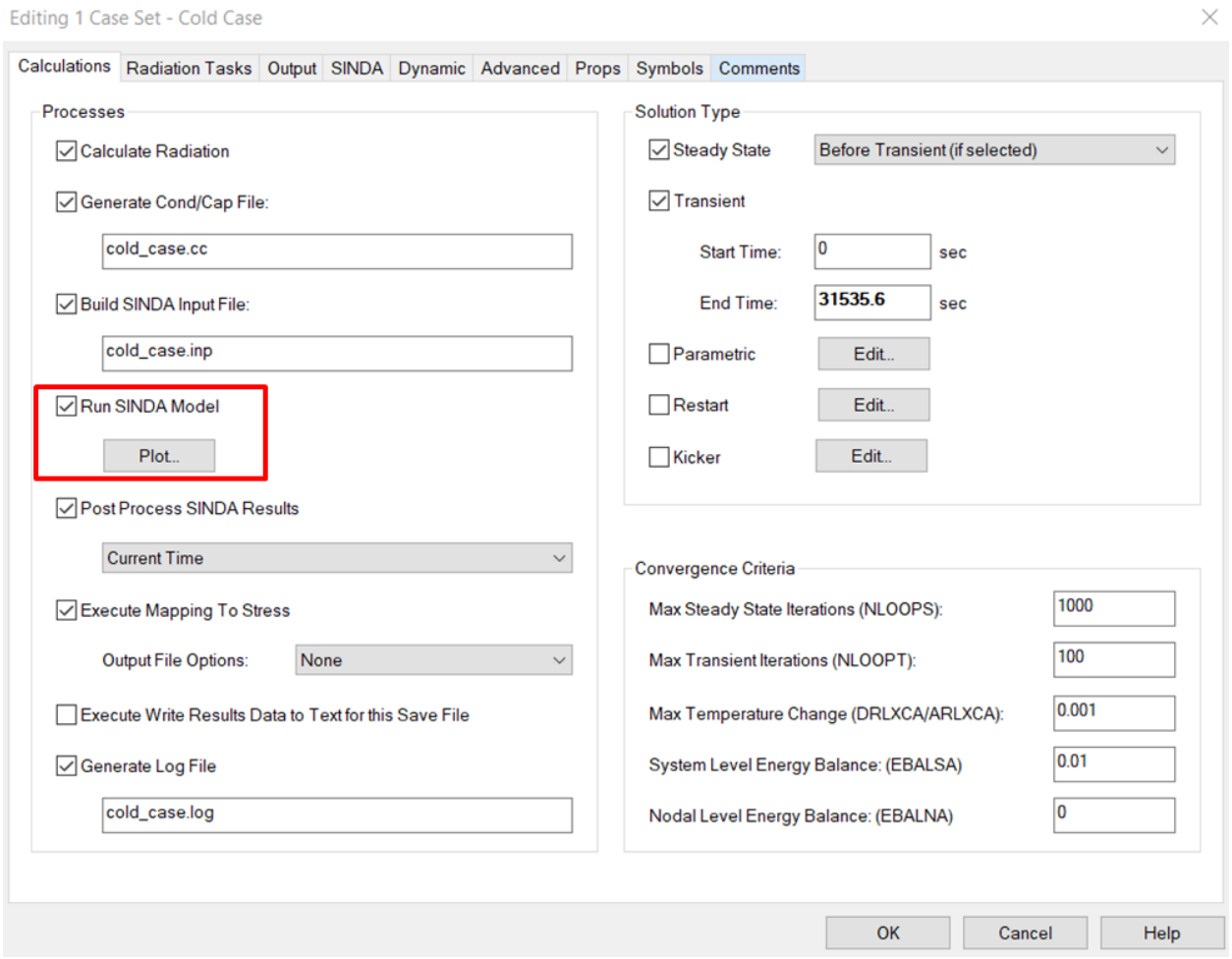


Figure 2-8: RUN SINDA options must be selected for each Case Set

Case sets must save results to a .sav file: CSR folders/directories cannot be used at this time to save SINDA results, and therefore only a save file can be used. Using CSR folders/directories will currently result in *Veritrek* not being able to find results for the desired node groups. This setting for using .sav files or CSR folders/directories can be found by navigating to the "Preferences" option of the Thermal tab, as see in Figure 2-9.

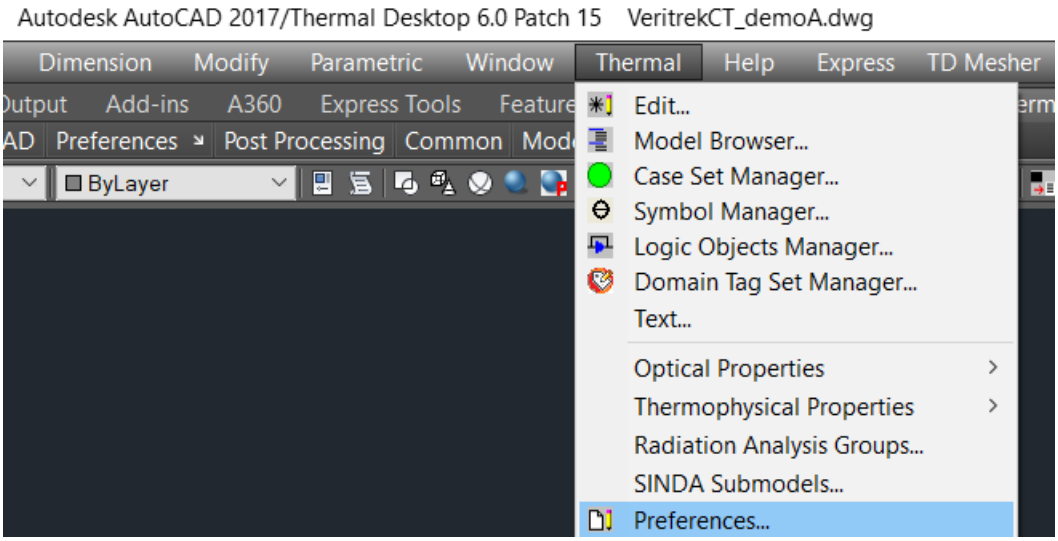


Figure 2-9: Preferences option from the Thermal tab

After this navigate to the SINDA tab and select the "Save File" option for the SINDA Results Format type, as seen in Figure 2-10.

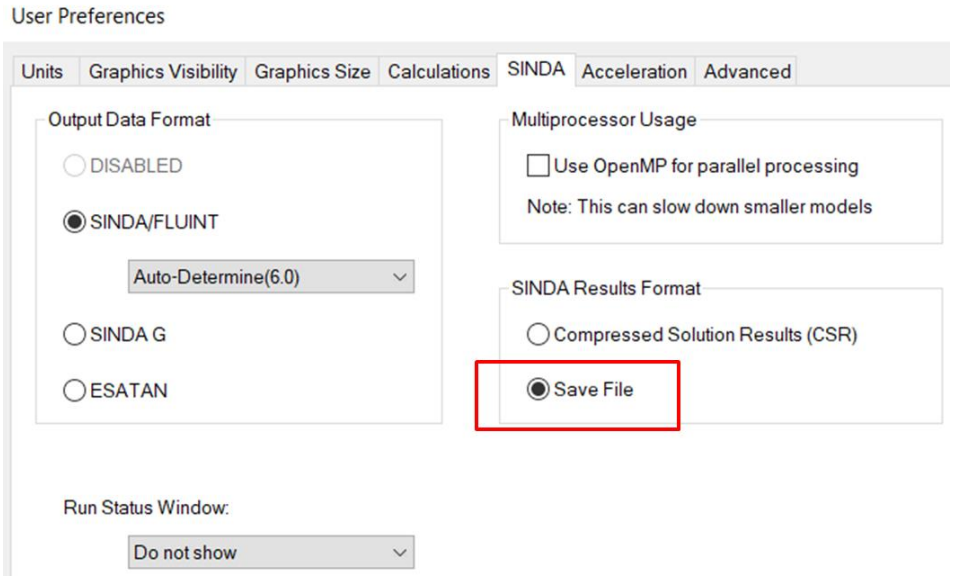


Figure 2-10: Save File option for the SINDA Results Format type

Lastly, verification of using .sav files and the correct set up of the .sav files is shown in the Output tab of a case set in Figure 2-11.

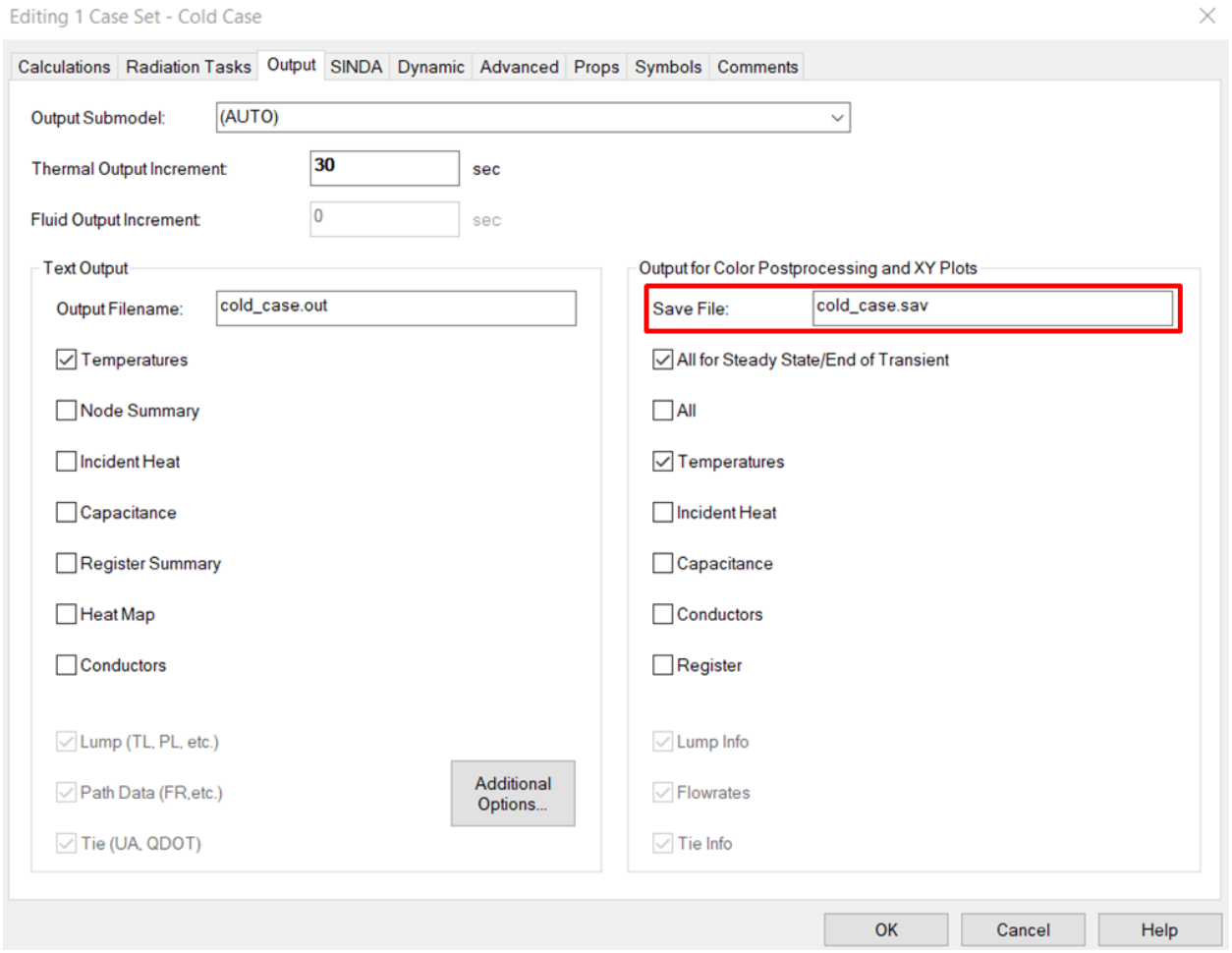


Figure 2-11: Results for each Case Set must be saved to a .sav file

Case sets must run in a user defined folder with the Case Set name: *Veritrek* currently requires the case sets to be run in a user defined directory that contains the same name as the case set. This setting can be found in the Advanced tab of a case set and is shown in Figure 2-12.

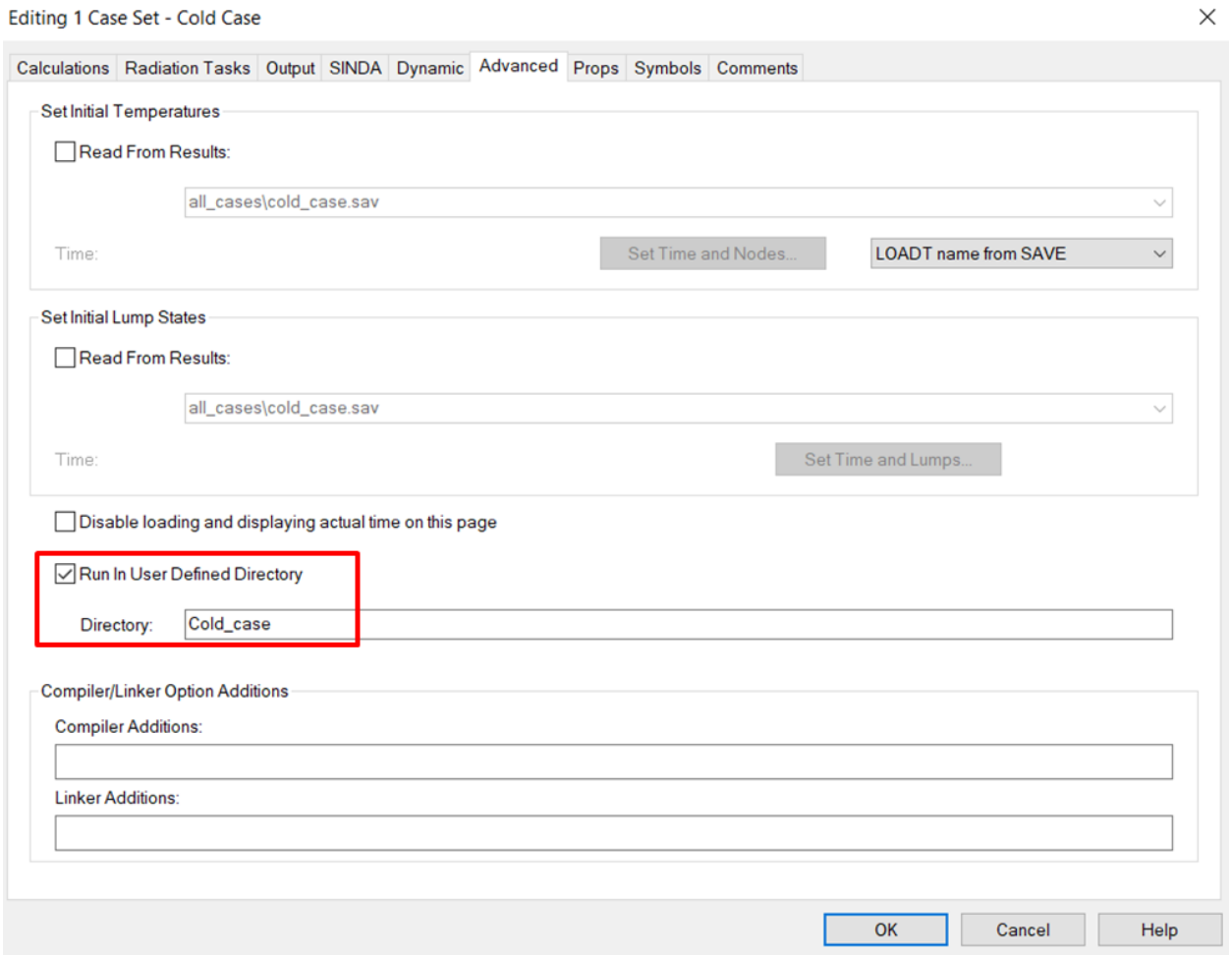


Figure 2-12: Each Case Set must run in a user defined folder with the Case Set name

Case sets cannot override symbols being used as an input factor: See Section 2.1 for more details.

Case sets must include Optical Properties and Thermophysical Properties overrides: *Veritrek* currently requires the case sets to include overrides for the .rco and .tdp files. This setting can be found in the Props tab of a case set and is shown in Figure 2-13.

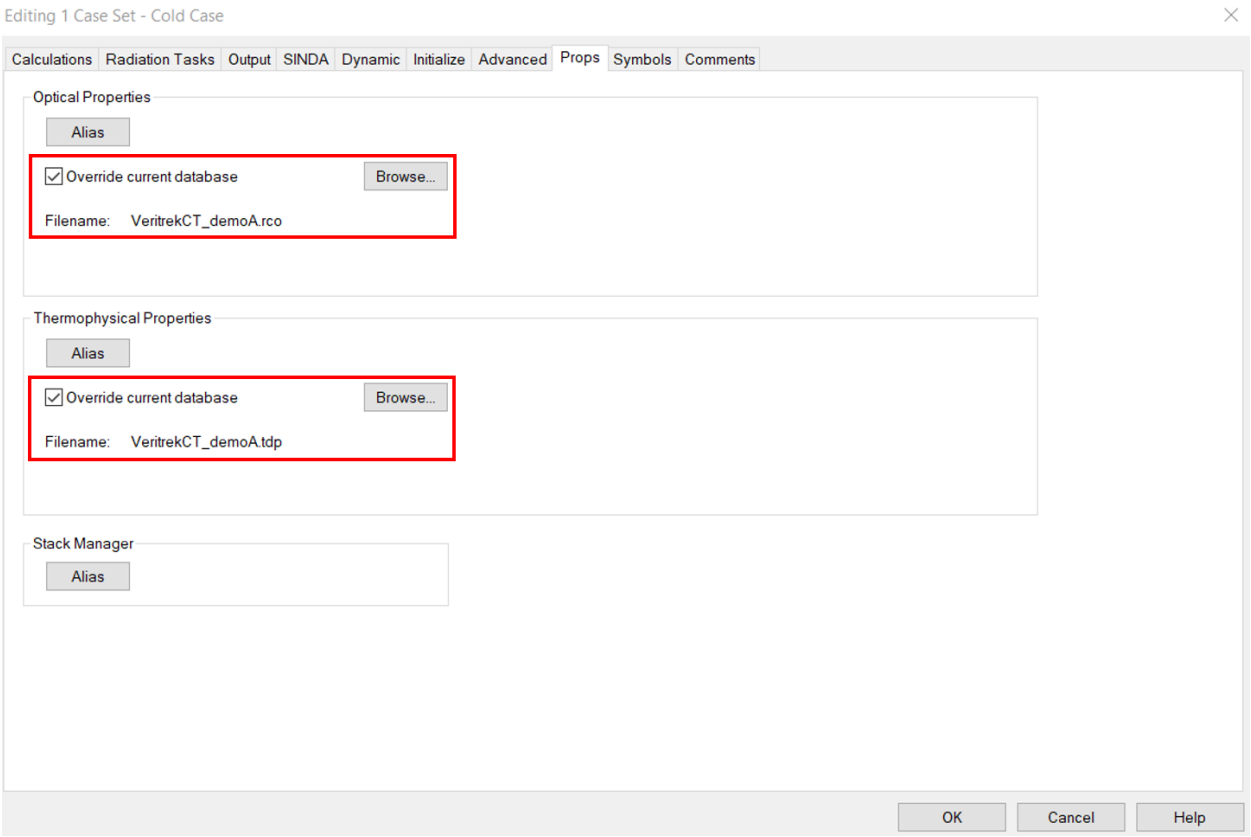


Figure 2-13: Each Case Set must include Optical Properties and Thermophysical Properties overrides

Enabling the AutoCAD Command Line: Before using the TD model with the *Veritrek Creation Tool*, it may be helpful in some circumstances to ensure that the AutoCAD command line is active and docked. If the command line is disabled, press CTRL-9 in the AutoCAD window. If the command line is undocked, it can be docked by moving it to the bottom of the AutoCAD window. Please consult the AutoCAD help document for more details.

2.4 TD Model Requirements for Using Registers in Veritrek

The following information represents some helpful tips in setting up the underlying TD model for successful *Veritrek* use, specifically if a user wants to use registers as an output response. These tips have come from interaction with users and can be looked at as solutions to frequently encountered issues regarding the necessary TD model settings.

2.4.1 How to set-up registers to work with *Veritrek*

All registers must be set up as TD Symbols that get exported as SINDA Registers: Most of the time, this is how registers are set up in TD anyways. However, there are some built in SINDA registers that act differently, and these too will need to be set-up as symbols by just inserting the register expression as the symbol's value. It is likely the result will show as "ERROR" in TD's symbols deck, but that is expected. An example of this is shown in Figure 2-14.

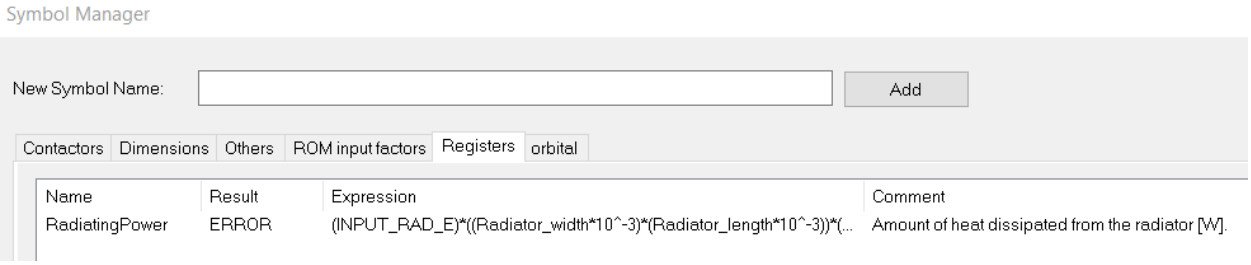


Figure 2-14: Registers must be set up as TD symbols organized into a "Registers" tab

After setting up the symbol and setting the symbol's value as a register expression, a user will need to click the "Control Symbol Output to SINDA Register…" button in the Expression Editor of TD's Symbol Manager, and make sure to check the option of having the symbol always output as a SINDA Register. These setting are shown in Figure 2-15.

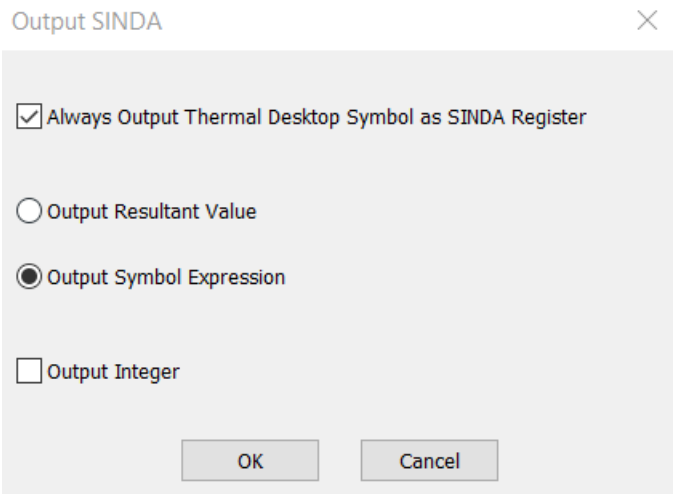


Figure 2-15: Symbols used as registers must be set to output as a SINDA Register

All registers must be organized into their own tab named "Registers" in the TD symbols deck: This organization technique is currently implemented to prevent confusion from selecting registers as an input factor. *Veritrek* specifically looks for the tab named "Registers" and omits this tab from the Inputs section, while also using all symbols in this "Registers" tab as registers available for selection in the Outputs tab of the *Veritrek Creation Tool*. An example of this is shown above in Figure 2-14.

Each Case Set used in *Veritrek* must be saving Registers to the .sav file: This option is in the Output tab in TD's Case Set Manager. For each output response type that will be used in a user's ROM creation, that option must be selected; and this must repeat for every case set to be used in a user's ROM creation, otherwise the output will be desensitized in the *Veritrek Creation Tool* and will not be allowed to select. A safe rule of thumb will be to select the "All" option. This setting is shown in Figure 2-16.

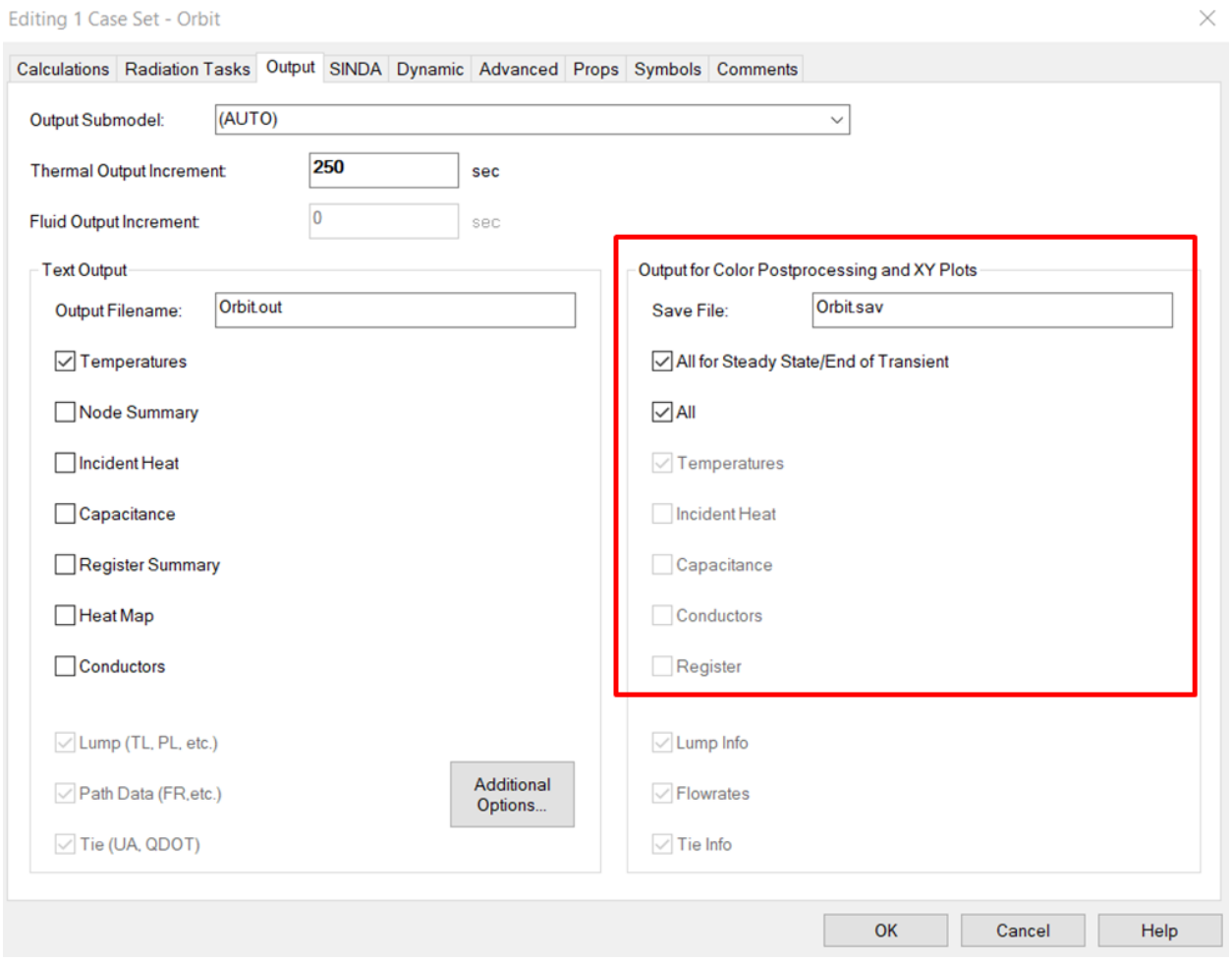


Figure 2-16: All desired output types need to be saved to the case sets .sav file

2.4.2 How to use registers to store QFLOW data for use in *Veritrek*

QFLOW data from ALL submodels to/from an individual node: If the heat flow to or from boundary node(s) interacting with all other nodes and submodels is of interest, a symbol can simply be set-up in the "Registers" tab of the symbols deck and be used to store the expression SUBMODEL.Q#, where "SUBMODEL" is replaced by the submodel name of the node of interest, and "#" is replaced by the node's number. This symbol can also be used to store an expression for Q's of multiple nodes, such as SUBMODEL.Q1+SUBMODEL.Q2+SUBMODEL.Q3.

*** Helpful Tip - Note that this set up only works for boundary nodes, not diffusion nodes. For an equivalent set up with diffusion nodes, see the next subsection on setting up logic objects.*

For example, in VeritrekCT_demoA, there is a boundary node set-up in a "BOUNDARY" submodel. To track the heat flow to/from this boundary node, a symbol was set-up in the "Registers" tab, "BOUNDARY.Q1" was used for the symbol expression, and the symbol was set to export to SINDA. This example can be seen in Figure 2-17.

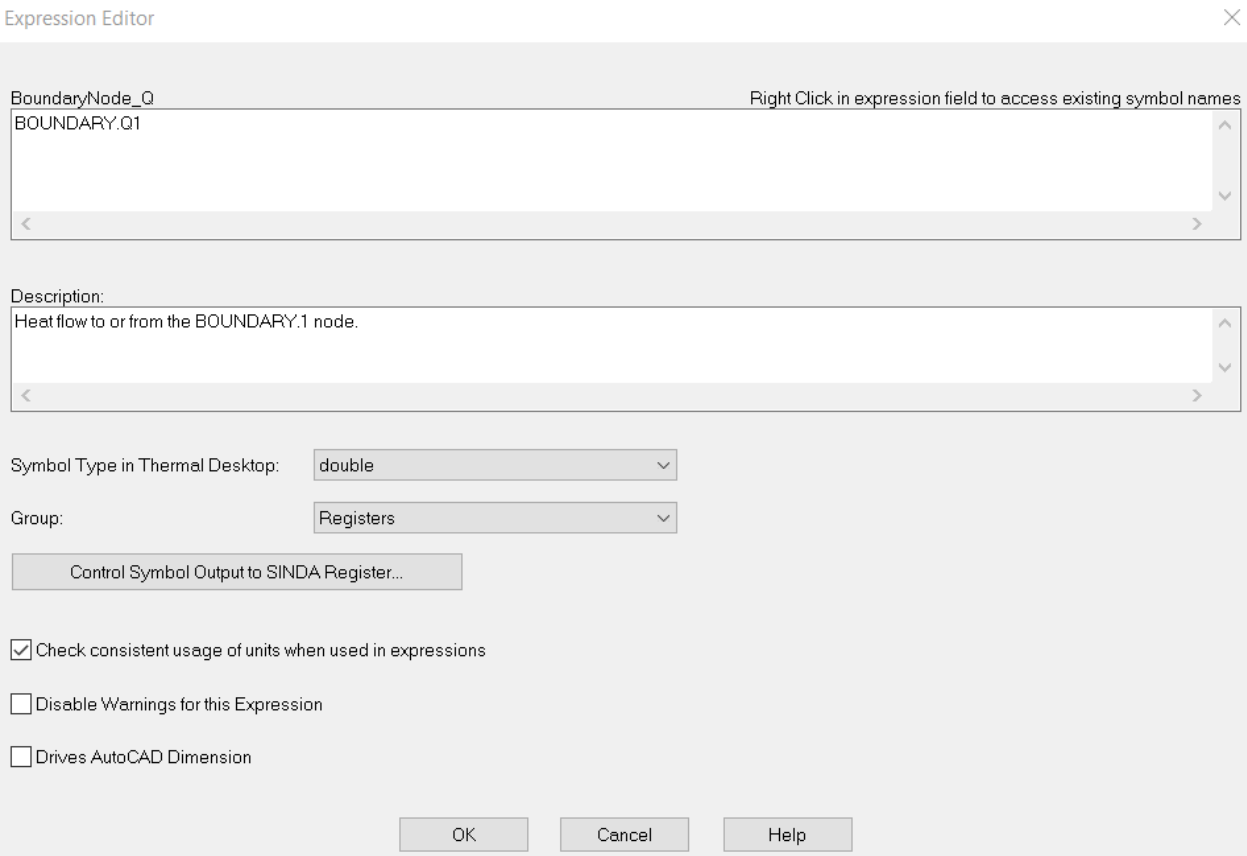


Figure 2-17: Store SUBMODEL.Q# as a register for tracking QFLOW data to/from an individual node

Set up "User Text Input HEADER/SUBROUTINE" logic objects to track QFLOW data for an array of nodes or to/from specific submodels: To track QFLOW data to/from an array of nodes or to/from specific submodels, user logic objects will need to be set-up along with registers that will be used to store the linear, radiative, and total heat flow.

First, in the "Registers" tab of the symbols deck, create three symbols. Use "0" for the expression of each of these symbols and be sure to export all three to SINDA. One symbol will be used to track the linear heat flow, the second symbol will be used to track the radiative heat flow, and the third symbol will be used to track the total heat flow. An example can be seen in Figure 2-18.

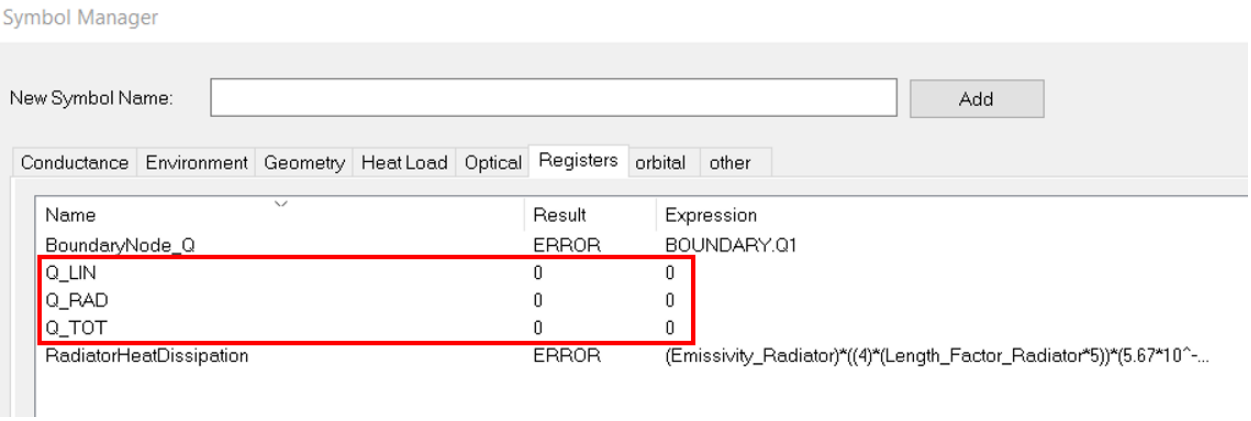


Figure 2-18: Set up three different symbols to track the linear, radiative, and total heat flow

Next, create the array of nodes you are interested in using the logic manager. Since the node IDs that are of interest for QFLOW are an array, you will have to create the user array manually as the "User Array" item will not work. Go into the Logic Manager and right-click to create a "User Text Input HEADER/SUBROUTINE." Choose the submodel name that you will use in the QFLOWSET routine and choose "ARRAY DATA BLOCK" for the "Code Place In" option. Enter the array as *array_id = node_id, node_id, node_id,* where *array_id* is the id you will use in QFLOWSET. Note that array data input lines must all be within the columns 2 through 1000 data field and may continue for as many lines as necessary. A comma at the end of the line is understood, even if it is not explicitly added. An example can be seen in Figure 2-19, where array 998 is being set up to group the PAYLOAD.1 and PAYLOAD.16 nodes.

Figure 2-19: Set up the array of nodes in the Logic Manager

Then, write the QFLOWSET call to dictate the "from" submodels or nodes, along with the "to" submodels or nodes for the heat flow of interest. Go into the Logic Manager and right-click to create a "User Text Input HEADER/SUBROUTINE." Leave (GLOBAL) as the submodel but place the code in "Operations Block Post Build (TDPOSTBL)". Then use the following command to call the QFLOWSET:

CALL QFLOWSET(#, 'FROM_SUBMODEL', FROM_NODE, 'TO_SUBMODEL', TO_ NODE)

Replace "#" with a unique identifier for the QFLOWSET, replace "FROM_SUBMODEL" with the name of the submodel that the "from" nodes are in, replace "FROM_NODE" with the node number or array

identifier of the “from” nodes, replace “TO_SUBMODEL” with the name of the submodel that the “to” nodes are in, and replace “TO_NODE” with the node number or array identified of the “to” nodes. Note that “0” can be used to dictate that all nodes of a submodel should be used. An example can be seen in Figure 2-20, where QFLOWSET 1 is being set up to track the heat flow from all nodes in the BUS submodel to the array of nodes in the PAYLOAD submodel that was set up in the previous step.

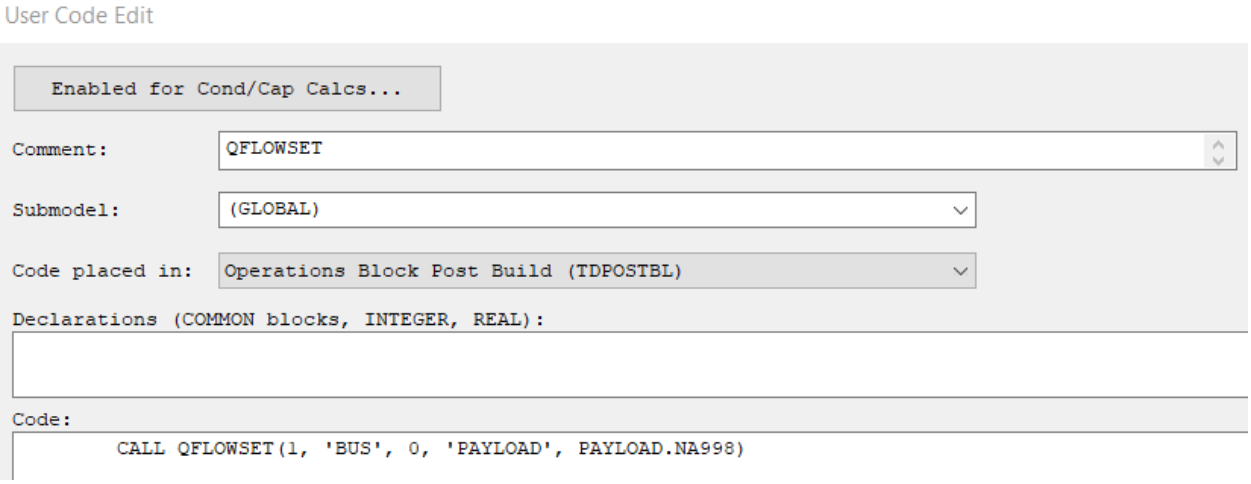


Figure 2-20: Set up the QFLOWSET call

Lastly, create the call to output the data from your QFLOSWET into the three registers that you setup in the first step. Go into the Logic Manager and right-click to create a “User Text Input HEADER/SUBROUTINE.” Leave (GLOBAL) as the submodel but place the code in “Output Calls.” Then use the following command to output the QFLOWSET data:

```
CALL QFLOW(#, REGISTER1, REGISTER2, REGISTER3)
```

Replace the “#” with the unique identifier you used for the QFLOWSET, replace “REGISTER1” with the name of the register that was set up to track the linear heat flow, replace “REGISTER2” with the name of the register that was set up to track the radiative heat flow, and replace “REGISTER3” with the name of the register that was set up to track the total heat flow. An example can be seen in Figure 2-21.

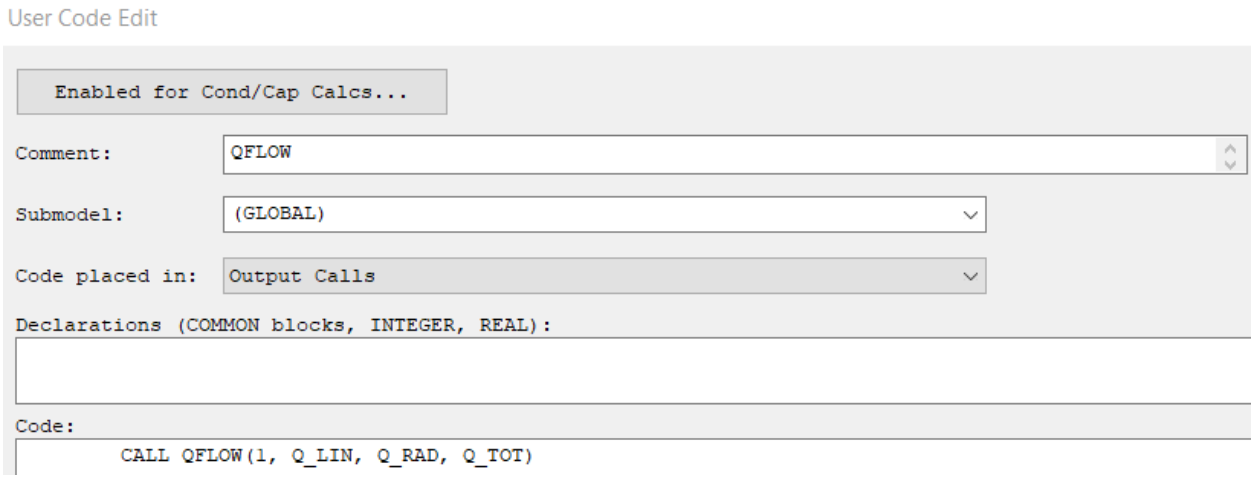


Figure 2-21: Set up the QFLOW call to output the data into registers

After creating these three logic objects, the Logic Manager should look like Figure 2-22.

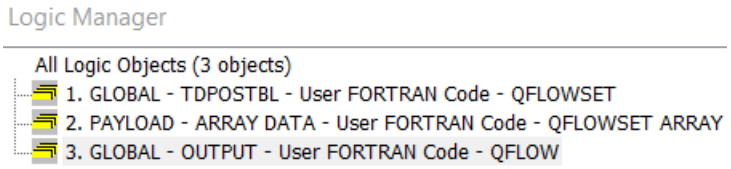


Figure 2-22: Set up the QFLOW call to output the data into registers

This will allow you to use registers to track QFLOW data for an array of nodes to/from a specific submodel. More information on syntax and best practice can be found in CRTech's SINDA Manual.

3 VERITREK CREATION TOOL OPERATION

Licensing and Installation Instructions can be found in the *Veritrek Installation Instructions Manual* that is sent with the license file. After installation is complete, the *Veritrek Creation Tool* can be opened by either using the shortcut icon that is automatically downloaded to the desktop, or by going into the \Program Files folder on the Local Disk drive. Inside of the \Program Files folder, there will be a \Creation Tool folder (which can be found nested inside of the \Veritrek folder) that will be the hub of any work that is performed using the tool. This \Creation Tool folder contains the actual tool's application, which when clicked will load and open the *Veritrek Creation Tool*. The \Creation Tool folder also contains a demo folder that contains the demo TD file that comes preloaded with the tool, python scripts and .dlls for the *Veritrek Creation Tool*'s sampling and data-fitting algorithms, and a help document that is this *Veritrek Creation Tool Users Manual*.

Inside of the higher-level \Veritrek folder, there is a folder for the Creation Tool that was just described, a \Exploration Tool folder that acts as the hub of any *Veritrek Exploration Tool* work, and a \License folder. The \License folder contains default Flexera license manager tools and batch files to ensure the most efficient and streamlined use of the tool on any platform. It is also important to note that the *Veritrek* license file gets placed into the \Veritrek folder that is in the \ProgramData folder on the Local Disk drive. For more information, please see the *Veritrek Installation Instructions Manual* that gets sent in tandem with the *Veritrek* license file.

Once the *Veritrek Creation Tool* is launched, the user is prompted to select the mode of operation they will be using: Full Feature License or Parallel Only License. The Full Feature License provides full capability of the Veritrek Creation Tool, while the Parallel Only License will only invoke the **ROM Creation Status** tab allowing a user to load an .lpxml file and just generate training data. A session can be started and is saved as a *Veritrek Creation Tool* ROM state file, which has the extension .lpxml. The *Veritrek Creation Tool* ROM state file contains the unique set of data to be used to create and test the ROM, which includes the nodes, symbols, and cases sets from the TD model; the user-selected input factors and output responses; the ROM sampling method and cases; the ROM data-fitting algorithm and associated input data; and the ROM testing method, simulations, and results. Adjacent to the .lpxml file is a "_temp" folder that will copy the .dwg file and associated property files for the *Veritrek Creation Tool* to use during ROM creation. This prevents any tampering with a user's underlying Thermal Desktop® model. The output from the *Veritrek Creation Tool* is a set of ROM files that contain the details and fitting parameters for the selected input factors and output responses. These ROM files are saved altogether in a folder, for easy import into the *Veritrek Exploration Tool* for data exploration.

The *Veritrek Creation Tool* interface (shown in Figure 3-1) is a tabbed interface, and the tabs are ordered so that progressing from top to bottom guides a user through the entire ROM creation process. The GUI will guide a user through the operations in order, enabling subsequent tabs as the necessary operations on the previous tabs are completed. There is also a simple toolbar at the top of the GUI that contains *File* and *Help* menus. The *File* menu allows a user to start a new ROM session, open a previously saved ROM

session, save their current ROM session, open a desired Thermal Desktop® model, or exit the tool. The *Help* menu provides documentation and other useful information and includes this *Veritrek Creation Tool Users Manual*. More detailed information on the File and Help menus can be found in Section 3.1.

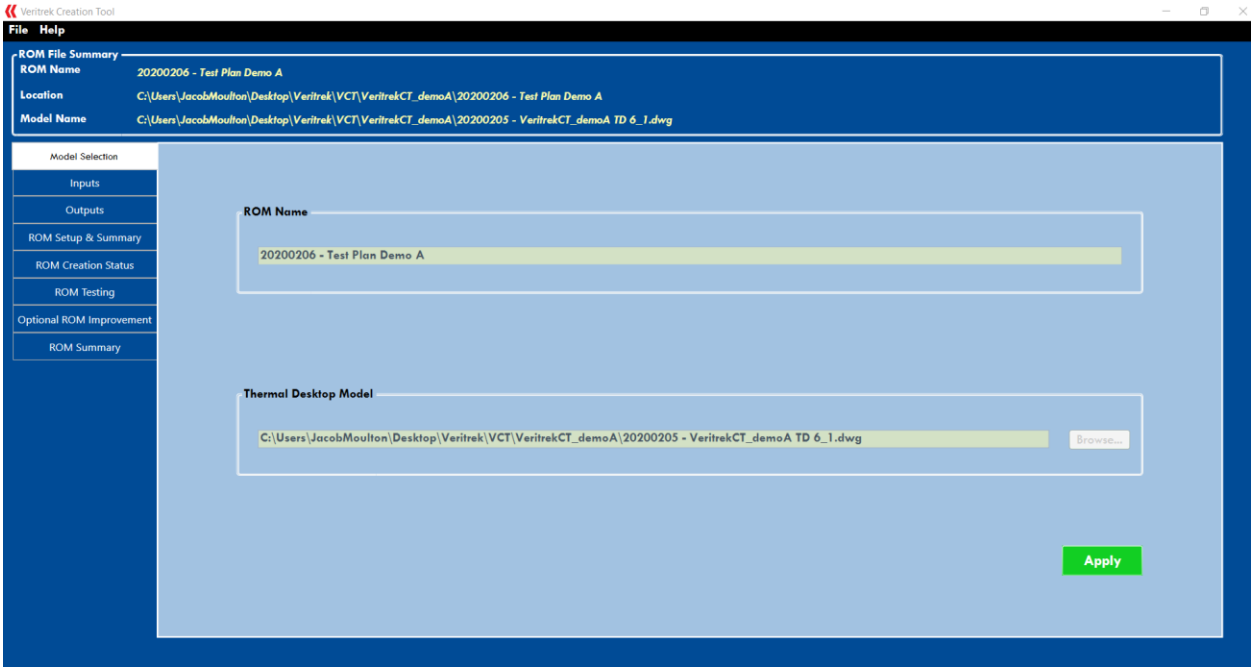


Figure 3-1: Main Window

In **Model Selection**, a ROM state file is associated with an underlying TD model. In **Inputs** and **Outputs**, the desired input factors and output responses are chosen for the ROM creation. In **ROM Setup & Summary**, the sampling and data-fitting algorithms are chosen, as well as the number of sample-runs to be used in the creation of the ROM. It is important to note that a recommended default minimum number of sample runs is chosen automatically based on the number and type of input factors but can be altered. A higher number of sample runs will yield better ROM results, but will most certainly take longer to create the ROM. In **ROM Creation**, the ROM is generated based on the parameters defined in the previous tabs. **ROM Testing** is used to test the ROM against a series of test runs performed within TD. **Optional ROM Improvement** allows for the improvement of a ROM by adding more sampling points, and **ROM Summary** summarizes the comparison results between the ROM and the TD model to describe the accuracy of the ROM. The following sections describe the GUI in more detail. More detailed information on the function and operation of these tabs can be found in Section 3.2 thru Section 3.8.

3.1 Main Toolbar

The Main Toolbar consists of the File and Help menus. Directly underneath the Main Toolbar is the ROM File Summary section, which stays visible regardless of the tab that is being worked. This ROM File Summary section contains the ROM name defined by the user, along with the location that the ROM is being saved in and the name of the underlying Thermal Desktop® model that the ROM is created from. Several different options are available from the File and Help dropdown menus, as is discussed in the next sections.

3.1.1 File Dropdown Menu

The *File* dropdown menu is shown in Figure 3-2. This menu contains the various operations that can be performed on the ROM session file, and one for TD. These operations can be invoked by clicking on the menu item or by using the shortcut keys that are defined for some of the commands.

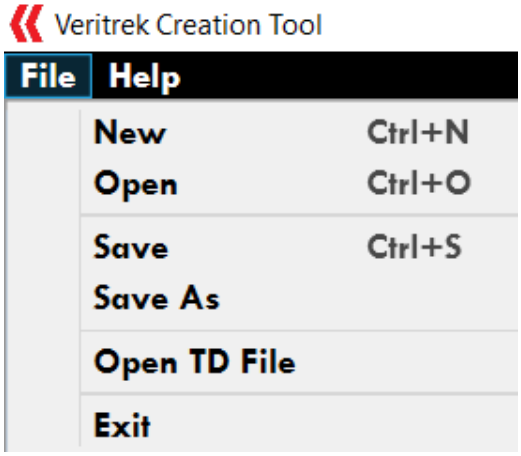


Figure 3-2: File dropdown menu

Selecting *New* creates a new and empty *Veritrek Creation Tool* ROM exactly as displayed in Figure 3-1. Selecting *Open* allows for the selection of an existing ROM session file (.lpxml). Selecting *Save* saves the current ROM session file. Selecting *Save As* allows the user to save the ROM session in another defined directory and with a new file name; however, note that changing the name will delete any data-fit associated with the current .lpxml file and should be used with caution. Selecting *Open TD File* opens the TD file that is currently being referenced by the ROM being created, in its last saved state. If there has not been a referenced TD file yet, an error message stating "No file Active" appears. Note that if the TD model is already open, selecting "Open TD File" does not open the model a second time. Selecting *Exit* closes the *Veritrek Creation Tool*.

3.1.2 Help Dropdown Menu

The *Help* dropdown menu is shown in Figure 3-3. This menu contains the various operations that can be used to assist the user or provide more information about the tool to the user.

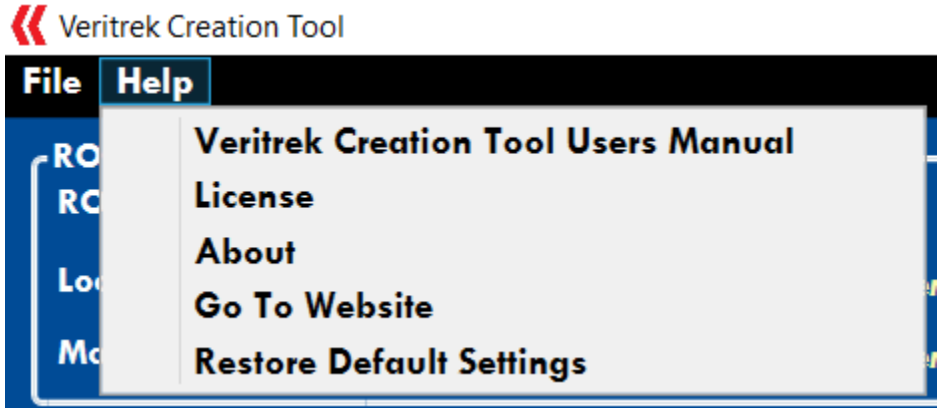


Figure 3-3: Help dropdown menu

Selecting *Veritrek Creation Tool Users Manual* opens this *Veritrek Creation Tool Users Manual*. Selecting *About* opens a window with the current version of the *Veritrek Creation Tool*, and information about which versions of AutoCAD and TD work with the current version of the *Veritrek Creation Tool*. Selecting License provides information on the status of the *Veritrek* license file that is being used to run the *Veritrek Creation Tool*. Selecting *Go To Website* opens a web browser to the home page of the Veritrek website at http://www.veritrek.com. Selecting *Restore Default Settings* allows all pop-up windows that a user saves as "Disable pop-up from appearing in the future", to start appearing again.

3.1.3 ROM File Summary section

The top panel of the *Veritrek Creation Tool* GUI shows a summary of the ROM name, location of the current ROM session file, and location of the referenced Thermal Desktop® model. These entries are fixed once they have been defined in the **Model Selection** tab and the ROM session file has been created. The ROM File Summary section is located directly underneath the Main Toolbar and is always visible throughout the use of the *Veritrek Creation Tool*. This section can be seen in Figure 3-4.

Figure 3-4: The ROM File Summary section

3.2 Model Selection

The first step in the ROM creation process is to complete the **Model Selection** tab, which can be seen in Figure 3-5. This tab invites the user to specify the name of the ROM that is to be created, select the reference Thermal Desktop® model file from which the ROM will be created, and click the *Apply* button. These three simple steps are described in more detail in the following sections.

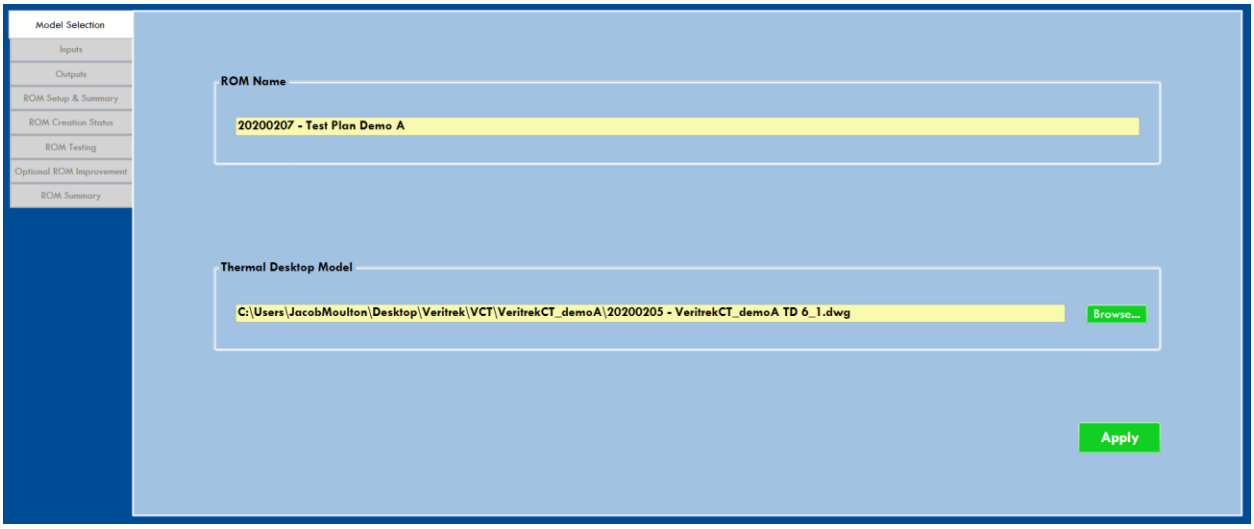


Figure 3-5: The Model Selection tab

3.2.1 ROM Name

To complete model selection, first a name for the current ROM needs to be entered in the space provided. It is important to note that after the ROM session file has been saved, the ROM name can only be changed by saving the ROM session file to a different name using *Save As* from the *File* menu.

*** Helpful Tip - It is also important to note that special characters should **NOT** be used in the ROM name, as this may cause reading and writing errors during the ROM creation process.*

3.2.2 Thermal Desktop® Model

Next, a TD model .dwg file with which to perform the ROM creation and analysis needs to be selected. A full filename can be manually entered in, or the .dwg file can be selected through a graphical file dialog by clicking on the *Browse…* button.

3.2.3 Apply

Once the ROM name and TD model have been defined, the *Apply* button needs to be selected. When *Apply* is selected, the *Save As* dialog appears to confirm the filename (the default filename is based on the ROM name entered) and location to save the ROM and prompts the user to save the newly created ROM session. At this point, all the necessary information is imported from the TD model selected into the *Veritrek Creation Tool*. This includes symbols, case set definitions, and nodes. It is important to note that the TD model to be used for the ROM analysis must not already be open during this operation. If it is already open, an error message will appear. The TD model will need to be closed out, and the *Apply* button in the *Veritrek Creation Tool* will need to be selected again. Once this is successfully completed, the *ROM File Summary* panel will be filled. In addition, the **Inputs** tab becomes activated.

The *Apply* button can also be used to update an opened ROM session file, should the TD model change. For an existing ROM session file, if the thermal model has changed and the *Apply* button is reselected, the user will be given the choice to update the *Veritrek Creation Tool* file to match the current state of the TD model.

*** Helpful Tip - After selecting "Yes" to this option of updating the TD model, the user will need to select the Apply button one more time, at which point a pop-up will appear saying that the model has been successfully updated.*

3.3 Inputs

Once the **Inputs** tab becomes activated, it can be selected and will look like Figure 3-6. In this tab, the user will select the TD symbols to include as input factors for the ROM generation. The symbols selected represent the variables that will be used to create the ROM in the *Veritrek Creation Tool* and used to define thermal analysis parameters during data exploration in the *Veritrek Exploration Tool*. After the input factors are selected, the input factor values to be included need to be defined. Case sets can then be chosen; and then lastly, the inputs selected and defined should all be checked. These steps are described in more detail in the following sections.

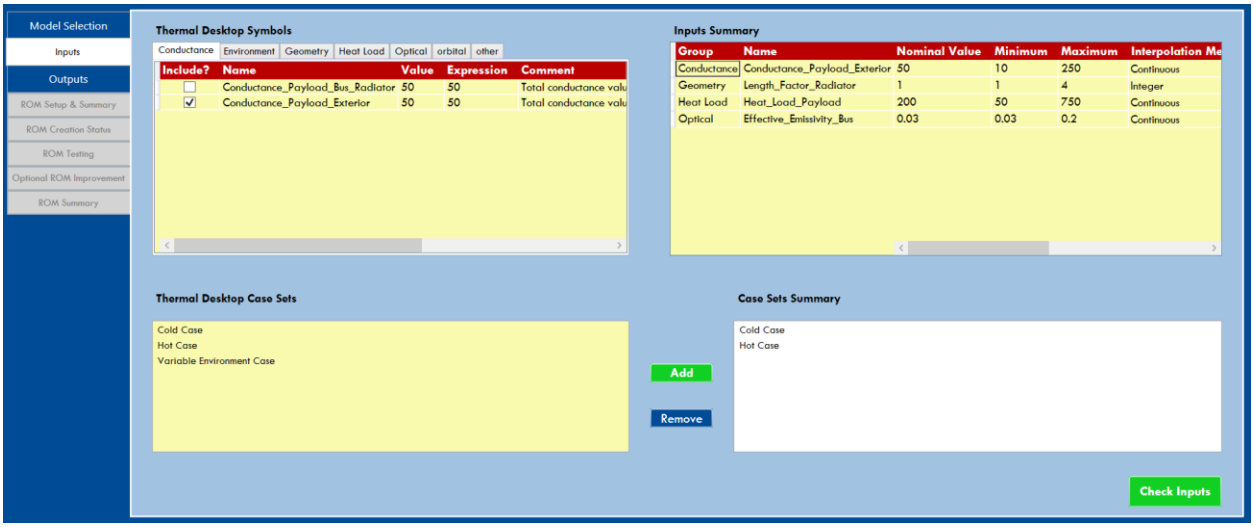


Figure 3-6: Inputs tab

3.3.1 Thermal Desktop® Symbols

The *Veritrek Creation Tool* creates a separate tab for each of the symbol groups defined in the referenced TD model. Each tab has a list of the symbols in that group arranged in a table, as shown in Figure 3-7.

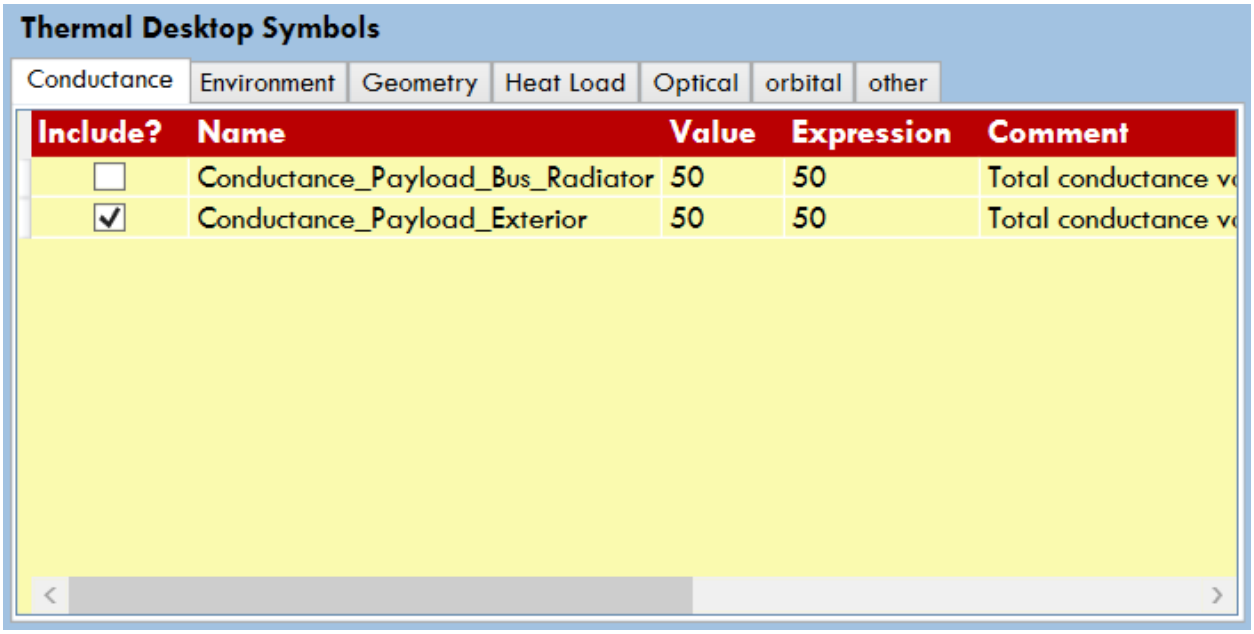
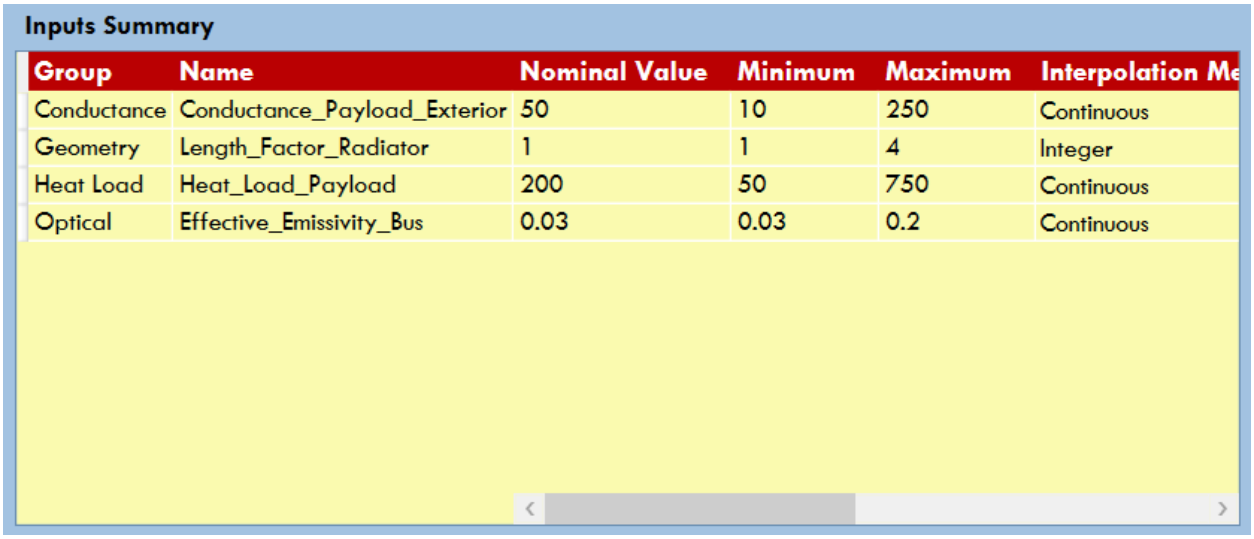


Figure 3-7: Thermal Desktop® Symbols section of the Inputs tab

The data in the "Name," "Value," "Expression," and "Comment" columns are defined in the TD model. To select a symbol as an input factor to be used in the ROM creation, click on the checkbox beside the variable name in the "Include?" column. At this point, the variable will appear in the Inputs Summary section. To remove a variable, simply uncheck the checkbox beside that variable name, or, in the Input Summary table, right-click and select "Remove input."

3.3.2 Inputs Summary

After selecting the input factors from the Thermal Desktop® Symbols section, the input factor type and design space range need to be defined in the Inputs Summary section, shown in Figure 3-8.



Group	Name	Nominal Value	Minimum	Maximum	Interpolation Me
Conductance	Conductance_Payload_Exterior	50	10	250	Continuous
Geometry	Length_Factor_Radiator	1	1	4	Integer
Heat Load	Heat_Load_Payload	200	50	750	Continuous
Optical	Effective_Emissivity_Bus	0.03	0.03	0.2	Continuous

Figure 3-8: Inputs Summary section of the Inputs tab

For each input factor, a minimum value, maximum value, and interpolation method need to be defined. To alter the default values, simply double-click on the desired entry and enter in a new value or select a different interpolation method.

*** Helpful Tip - It is important to note that the range of values for the input factor, going from minimum to maximum, will be the design space that gets sampled. Therefore, it is imperative to try and avoid extreme values for input factors. For example, although a desired range for Conductance may effectively be from 0 to 250 W/K, inserting 0 as the minimum value will be detrimental to the ROM creation process because Thermal Desktop® will try and perform a run with a conductance value of 0 W/K, which it cannot do. As a result, careful thought needs to be given when defining the range over which input factor values will be investigated, to effectively include a large design space efficiently and without errors.*

*** Helpful Tip – It is also important to note that, in general, ROM performance tends to not be as accurate at the very edges of the design space. Therefore, it is recommended to manually enter in a design space range that slightly exceeds the desired range for the input factor. For example, if a design space of .05 to .15 is desired for an effective emissivity, it is best to set the minimum and maximum values to .03 and 0.2 respectively to manually build in this buffer around the edges of the design space. If this does not conflict with the first tip described above, this will be a good standard practice.*

There are three interpolation methods to choose from for each input factor. The input factor can be defined as a Continuous input factor, an Integer categorical input factor, or a MinMax categorical input factor. The Continuous method specifies that any real value between the minimum and maximum values may be used, and therefore the minimum and maximum values do not have any restrictions other than that the minimum must be less than the maximum. The Integer method uses any integer value between the maximum and minimum values; therefore, the minimum and maximum values must be integers and

the minimum must be less than the maximum. The MinMax method uses only the minimum and maximum values, which must both be integers and the minimum must be less than the maximum.

3.3.3 Thermal Desktop® Case Sets and Case Set Summary

To complete the **Inputs** tab, at least one case set need to be selected. It is important to note that during ROM creation, each case set becomes another categorical input factor. Multiple case sets can be selected at the same time with the use of Ctrl+left mouse button or Shift+left mouse button. Once the desired case sets are selected, click the *Add* button to move them from the Thermal Desktop® Case Sets field to the Case Sets Summary field. To remove case sets from the Case Sets Summary field, select the sets to be removed and click the *Remove* button. As with selecting case sets to add, multiple case sets can be removed simultaneously with the use of Ctrl+left mouse button or Shift+left mouse button.

3.3.4 Difference between Continuous and Categorical Input Factors

Included in Veritrek's ROM definition is the distinction between two types of input factors: continuous and categorical. Continuous input factors are those selected to use the continuous interpolation method. Categorical input factors are those selected to use the MinMax and Integer interpolation methods, along with Case Sets. The key important distinction between these two is that Veritrek creates a category for each value of a categorical input factor and creates a sampled design space of all continuous input factors within each category. This results in the exact same sampling points and training runs, based off the sampled continuous input factors, being performed for each category such that each categorical input factor can be thought of as being run discretely. This also means that a ROM cannot be developed with only categorical input factors, as there would be nothing for the ROM to predict or interpolate.

The best way to visualize this is with an example. Take for instance the four input factors shown in Figure 3-8, along with two case sets also being selected. With two case sets, and an additional categorical input factor with four values (Integer interpolation method type from 1 to 4 for the Length_Factor_Radiator input factor), the result is 8 categories (2*4). The three continuous input factors will be identically sampled within each of these 8 categories based on the user-defined number of samples for the continuous input factor design space as discussed in Section 3.5. An image depicting this is shown in Figure 3-9.

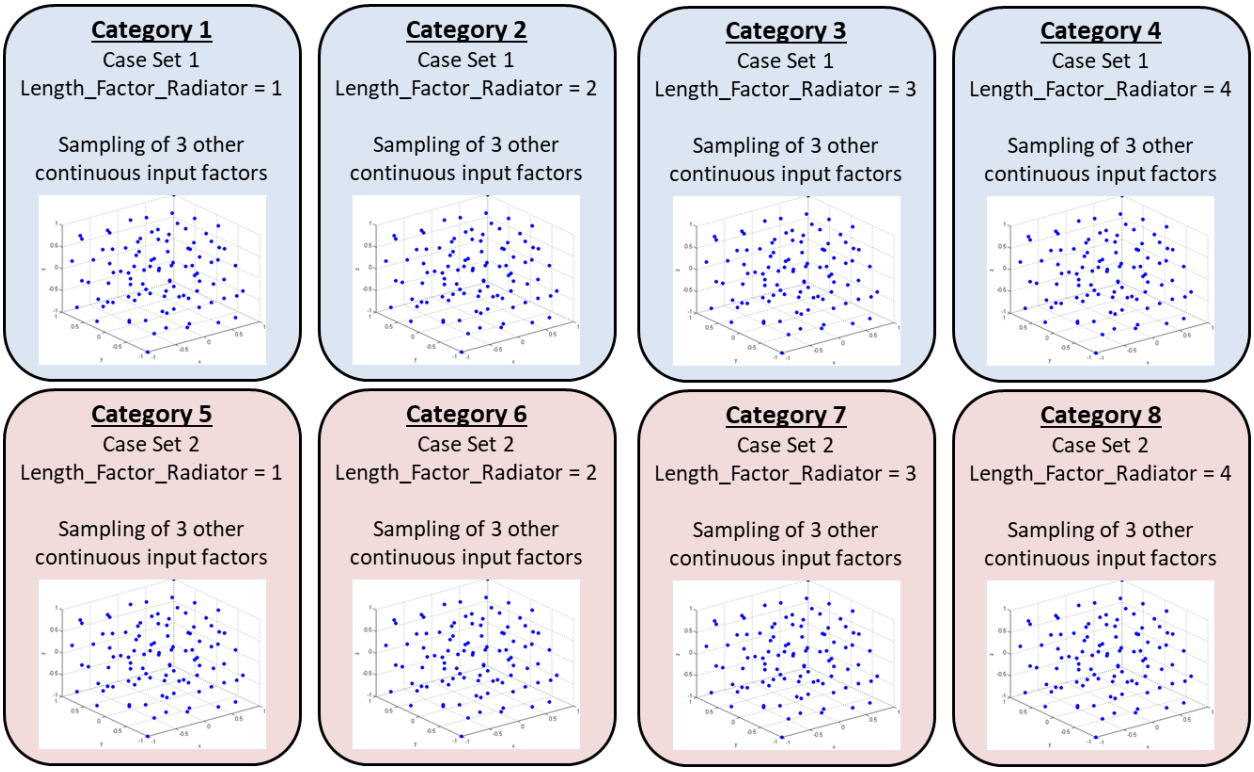


Figure 3-9: Depiction of Categorical vs. Continuous Input Factors

This distinction also comes into play during the **ROM Setup & Summary** tab, as the number of categories is shown as the "Categorical Combinations" and the number of sampled continuous input factors is shown as "# Training Runs/Category" in Figure 3-17.

3.3.5 Check Inputs button

Once the input factors are set up as desired, *Check Inputs* needs to be clicked to check that all input factors and their values are set up properly. When this button is selected, the *Veritrek Creation Tool* verifies that the inputs are chosen properly and that nothing is missing. If something is not correctly filled out, a pop-up will appear stating what needs to be changed. If everything is filled out properly, the *Veritrek Creation Tool* will give notification that the inputs are complete. At this point, the **Outputs** tab will become activated.

3.4 Outputs

Once the **Outputs** tab becomes activated, it can be selected and will look like Figure 3-10. In this step, the characteristics of nodes, groups of nodes, or registers will be selected as the output responses for the ROM. Currently, output responses include minimum, mean, and/0 maximum temperatures or incident heat values for nodes or node groups, along with minimum, mean, and/or maximum values for registers. First, nodes, node groups, and/or registers are selected and then output responses associated with those selections are determined. These steps are described in more detail in the following sections.

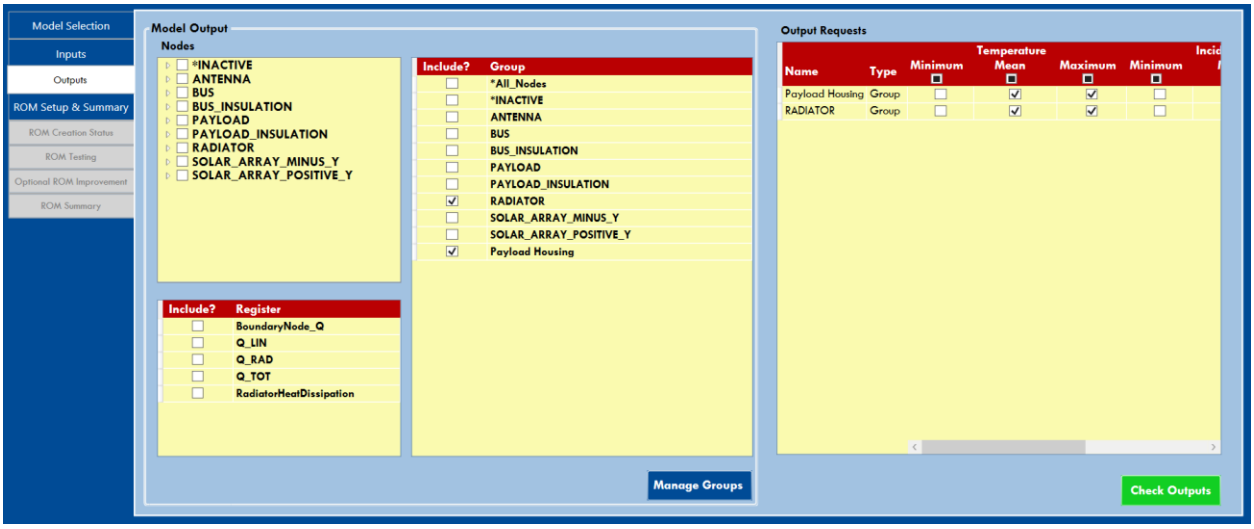


Figure 3-10: The Outputs tab

3.4.1 Model Outputs

The Model Outputs section is where individual node(s), node group(s), and/or register(s) of interest are selected for ROM creation. The Nodes section provides a list of all thermal nodes in the TD model, organized by submodel, as seen in Figure 3-11.

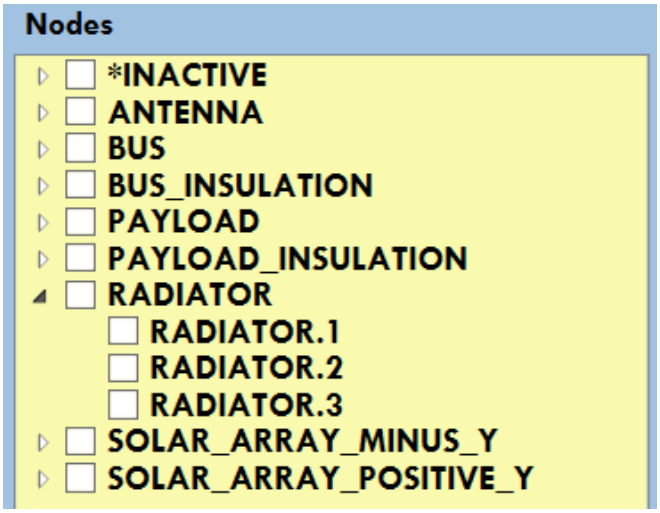
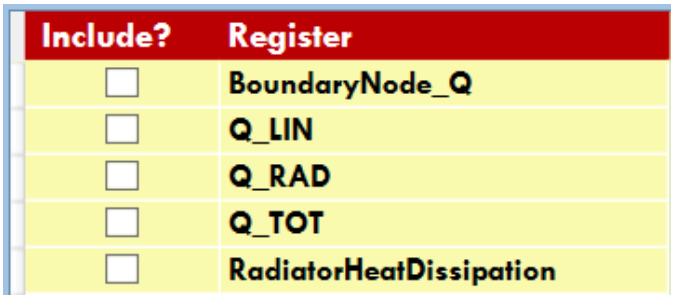


Figure 3-11: Nodes section of the Outputs tab

Each submodel has a checkbox that is empty by default, along with a collapsible button that expands the submodel to show each individual node. All thermal nodes within a submodel can be selected by clicking the checkbox beside the submodel. If only certain nodes within a submodel are desired, simply expand the node list for that submodel and select the node or nodes. Once a node is selected, it is listed in the Output Requests section. A node or submodel can be removed from the Output Requests section by unchecking the checkbox beside the item, or by right clicking the output in the Output Requests section and selecting “Remove output request.”

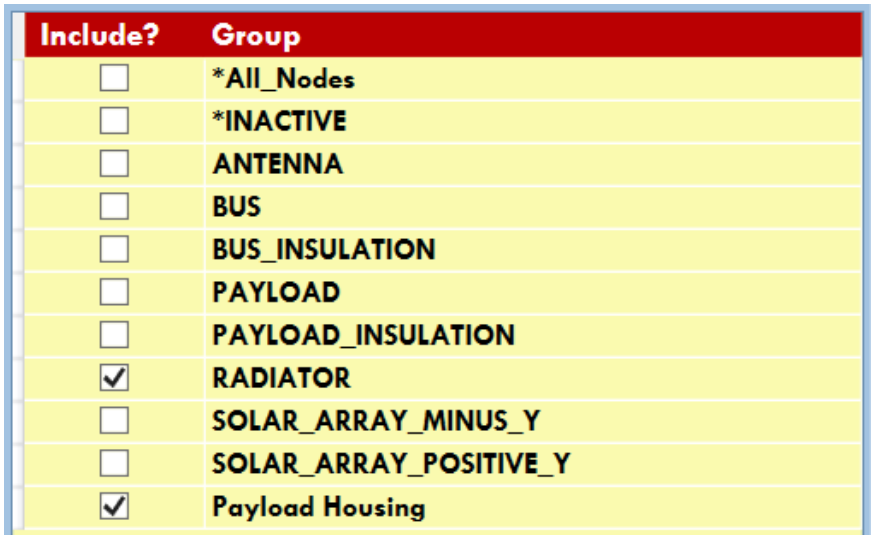
The Registers section provides a list of all registers that the *Veritrek Creation Tool* imported from the Registers tab set-up in the user's Thermal Desktop® model, as seen in Figure 3-12. For instructions of how to properly set-up registers such that they show up in the *Veritrek Creation Tool*, refer to Section 2.4. Each register has a checkbox that is empty by default. You can select the register by clicking the checkbox. Once a register is selected, it is listed in the Output Requests section. A node group can be removed from the Output Requests section by unchecking the checkbox beside the item.



Include?	Register
☐	BoundaryNode_Q
☐	Q_LIN
☐	Q_RAD
☐	Q_TOT
☐	RadiatorHeatDissipation

Figure 3-12: Registers section of the Outputs tab

The Node Group section provides a list of all groups that the *Veritrek Creation Tool* created from the TD model, as seen in Figure 3-13. It is important to recognize the difference between selecting from the Nodes section and the Node Group section. Selecting from the Node Group section allocates a single output response for the entire node group. For example, maximum temperature for the RADIATOR node group will give a single temperature value that represents the maximum of any RADIATOR node. In this example, the single value returned will be the highest temperature out of any node contained within the RADIATOR node group. However, selecting from the Nodes section allocates a single output response to an individual node. For example, maximum temperature for the RADIATOR.1 node will give the maximum temperature for this individual node.



Include?	Group
☐	*All_Nodes
☐	*INACTIVE
☐	ANTENNA
☐	BUS
☐	BUS_INSULATION
☐	PAYLOAD
☐	PAYLOAD_INSULATION
☑	RADIATOR
☐	SOLAR_ARRAY_MINUS_Y
☐	SOLAR_ARRAY_POSITIVE_Y
☑	Payload Housing

Figure 3-13: Node Group section of the Outputs tab

Each node group has a checkbox that is empty by default. You can select the node group by clicking the checkbox. Right-clicking on the node group and selecting “Add group nodes as output requests” is another way of selecting a node group for an output response. Once a node group is selected, it is listed in the Output Requests section. A node group can be removed from the Output Requests section by unchecking the checkbox beside the item, or by right clicking the output in the Output Requests section and selecting “Remove output request.” Also, a node group can be removed from the Output Requests section by right clicking the group in the Node Group section and selecting “Remove group nodes from output requests.”

By default, node groups are automatically generated based on the thermal submodels that are present in the Thermal Desktop® model. However, the user may be interested in a unique set of nodes as a node group. The Manage Groups option can be used to create a unique node group. Clicking the *Manage Groups* button, at the bottom of the Model Output section, opens the Manage Groups GUI, shown in Figure 3-14. This GUI allows a user to create a new node group based on individual nodes. Node groups can also be imported from a .txt file and/or exported to a .txt file using this feature.

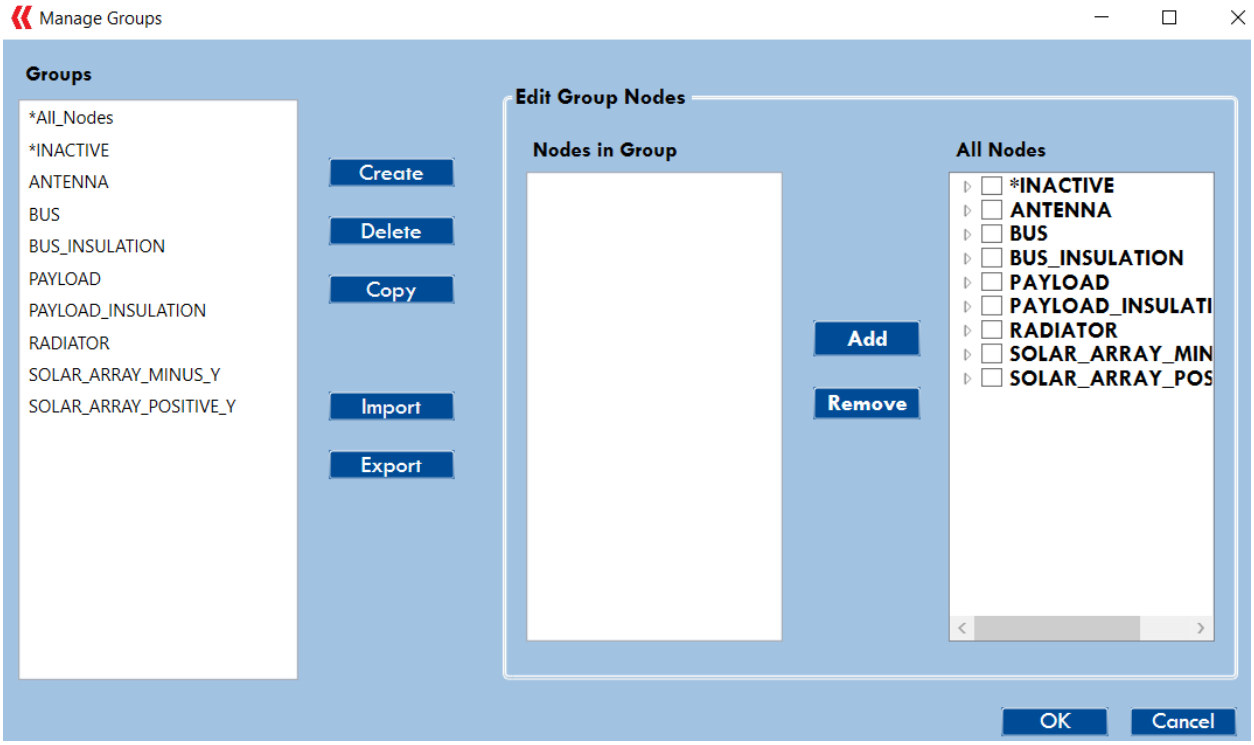


Figure 3-14: The Manage Groups GUI

To create a new group, press *Create* and then type in the desired group name in the text box and click *OK*. The new group will be displayed in the Groups list on the left side of the GUI shown in Figure 3-14. Node groups displayed on the left side of the GUI can be selected, and the nodes included in the selected group will appear in the middle pane titled Nodes in Group. These node groups on the left side can be deleted by selecting and pressing *Delete*, they can be copied by selecting and pressing *Copy* or they can be renamed by double-clicking on the node group name and typing in a new name.

The node groups on the left side can also be edited by selecting and either adding or removing nodes, as shown in Figure 3-15. The center pane shows the nodes currently in the selected node group. Nodes can be added to the selected node group by selecting a node from the pane at the right, titled All Nodes, and clicking Add.

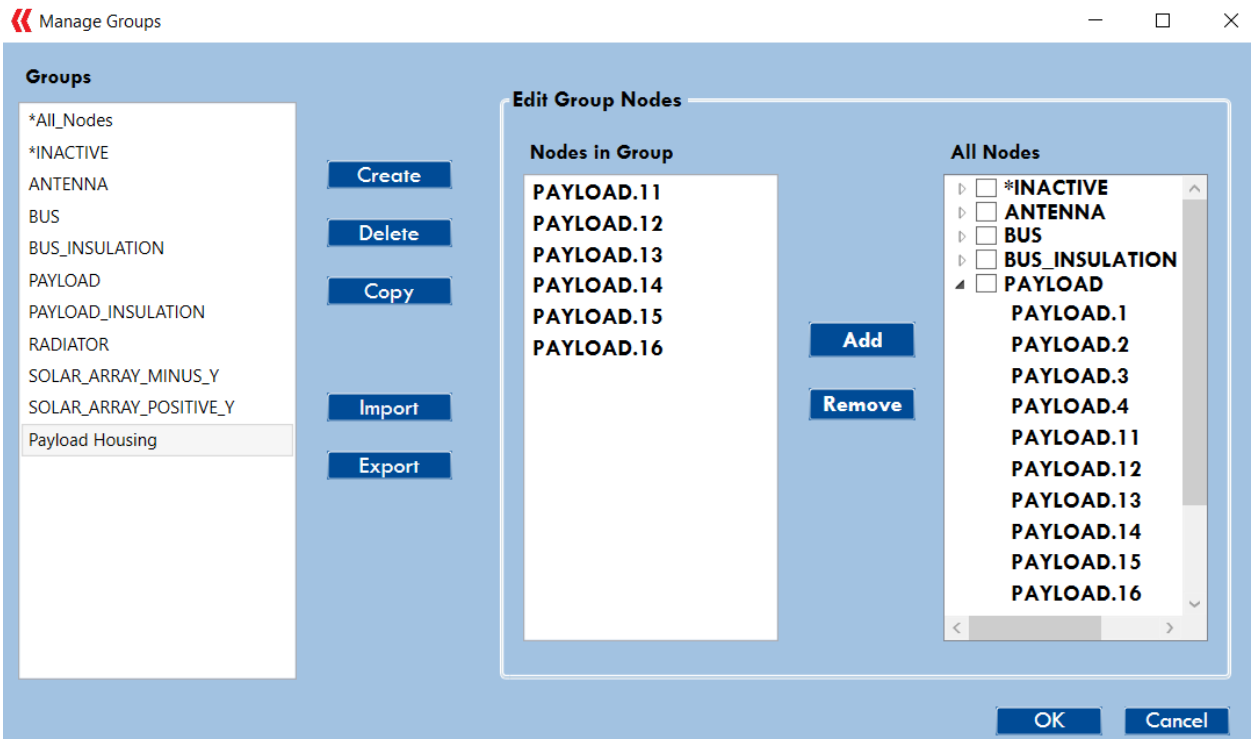


Figure 3-15: Editing Node Groups using the Manage Groups feature

To import a group from a text file, press *Import*. A graphical file dialog will appear. Select the text file and press *Open*. Enter a name for the node group and press *OK* to import. The text file must contain a list of nodes in the format of SUBMODEL.NODE_ID, one node per line. The best way to understand the format is to export a group and view the resulting text file. To export a group to a text file, press *Export*. A graphical file dialog will appear. Enter the name of the text file and press *Save*. The text file will write each node to a separate line in the file using the SUBMODEL.NODE_ID format.

Once the user is finished creating or editing node groups, simply click *OK* and the Node Groups section in the Model Output section will be updated.

3.4.2 Output Requests

The Output Requests section lists all the nodes and/or node groups selected from the Model Output section in the previous step, an example of which is shown in Figure 3-16.

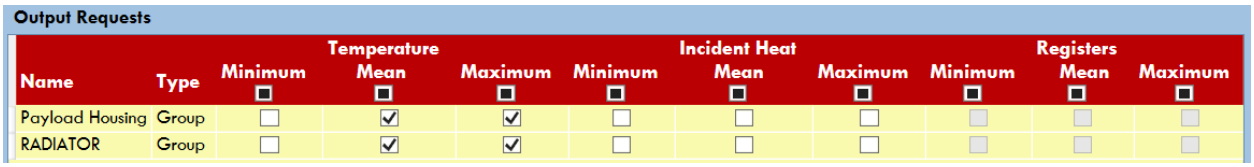


Figure 3-16: Output Requests section of the Outputs tab

The Output Requests table consists of the following columns: "Name," "Type," "Minimum Temperature," "Mean Temperature," "Maximum Temperature," "Minimum Incident Heat," "Mean Incident Heat," "Maximum Incident Heat," "Minimum Registers," "Mean Registers," "Maximum Registers." All rows in the "Minimum," "Mean," and "Maximum" columns' checkboxes are blank by default. At least one output type for each node, node group, and register listed in this table needs to be selected. To select a given output type for all the listed outputs, check or uncheck the checkbox directly under "Minimum," "Mean," or "Maximum." This will modify all checkboxes in that column.

3.4.3 Check Outputs button

Once the output responses are set up as desired, *Check Outputs* needs to be clicked to check that they were set up properly and nothing is missing. If something is missing or incorrect, a pop-up will appear stating what needs to be changed. If everything is filled out properly, the *Veritrek Creation Tool* will give notification that the outputs are complete. At this point, the **ROM Setup & Summary** tab will become activated.

3.5 ROM Setup & Summary

Once the **ROM Setup & Summary** tab becomes activated, it can be selected and will look like Figure 3-17. This is the tab that sets up and summarizes the ROM Creation. The sampling and data-fitting algorithms are selected. Currently, the only available option for the sampling algorithm is a Latin Hypercube Sampling Algorithm designed by LoadPath, which includes a Maximin optimization scheme to most effectively sample the total design space defined by the input factors. Likewise, the only currently available option for a data-fitting algorithm is a Gaussian Process algorithm designed by LoadPath, which includes hyperparameter optimization schemes to fit the ROM data most effectively between the generated training data points. Also, in the **ROM Setup & Summary tab**, the total number of runs is determined by multiplying the Categorical Combinations value by the user-specified Number of Runs/Category value. A default minimum Number of Runs/Category value is entered based upon the number of categorical and continuous input factors that are chosen; however, this value can be altered manually. It is important to note that increasing this value will result in a more accurate ROM, but it will take longer to create. This is a trade-off and balance that the user will have to weigh for their ROM and ROM needs. These steps are described in more detail in the following sections.

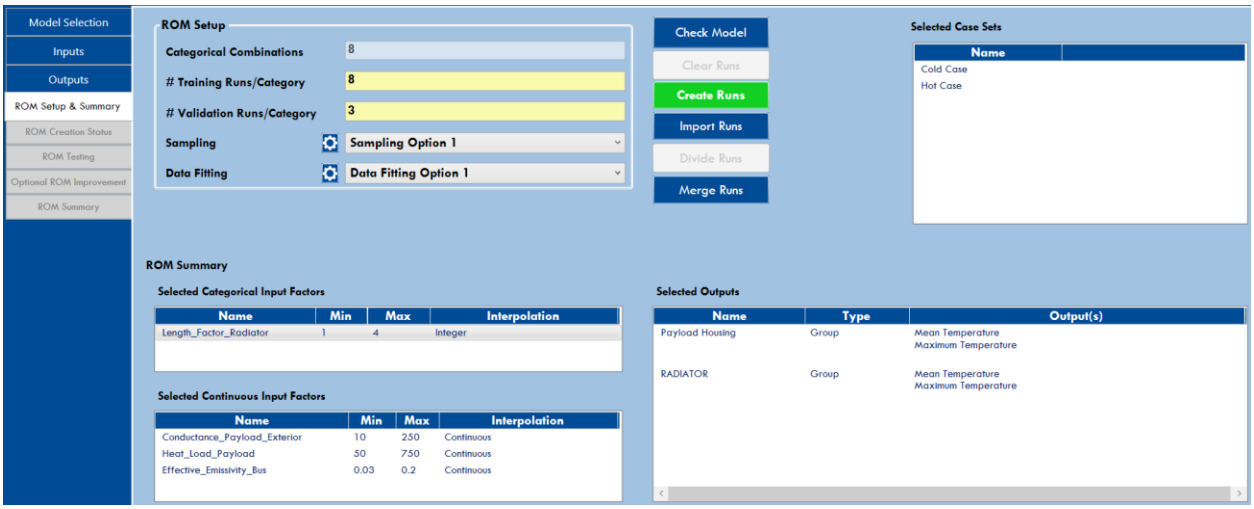


Figure 3-17: The ROM Setup & Summary tab

3.5.1 Check Model

When first navigating to the **ROM Setup & Summary** tab after filling in **Inputs** and **Outputs**, it is required for the *Veritrek Creation Tool* to check the referenced Thermal Desktop® file before continuing. This step reloads the contents of the TD model to make sure that the symbols, case sets, and outputs defined in the *Veritrek Creation Tool* have not changed.

Once the check is complete, TD closes and a pop-up appears stating that "ROM passed model checks". At this point, the ROM has passed model checks and the *Create Runs* button becomes activated. If the model does not pass the model checks, this means that the ROM session file does not match the TD file, which is most likely due to an updated TD file. To update the ROM session file, go back to the **Model Selection** tab and click the *Apply* button again. Updates may then need to be made to the **Inputs** and **Outputs** tabs, depending on the TD model changes.

3.5.2 ROM Setup

The next step is to fill out the ROM Setup section. The Categorical Combinations value is automatically determined and set. This value is based on the case sets and the categorical input factors chosen in the **Inputs** tab. Categorical input factors are those that have been defined by the MinMax or Integer interpolation methods. The Categorical Combinations value is the product of the number of case-sets and the number of values for each of the categorical symbols. For input factors with the MinMax interpolation method, there are only two values; but for the Integer interpolation method, the number of values is equal to the difference between the maximum and minimum values.

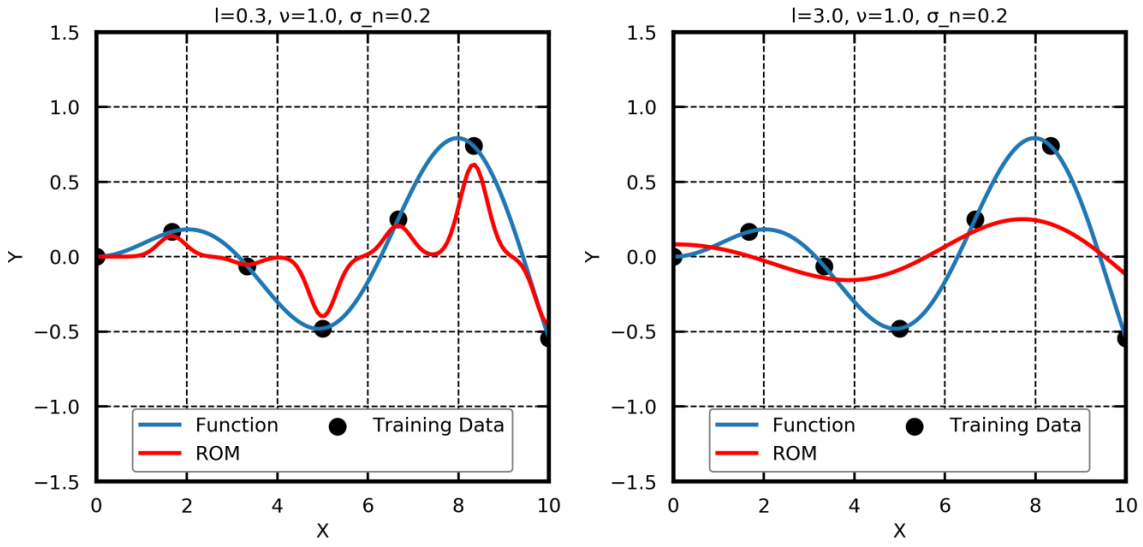
The # Training Runs/Category value is a default recommended minimum set based on the number of continuous input factors. The recommended value is determined by 2^n, where n is the number of continuous input factors. However, this value can be altered to a user-defined value. It is important to note that increasing this value may result in a more accurate ROM, but it will take longer to create because the total number of runs created is the product of the Categorical Combinations value and the total # Runs/Category value. The default value is a general guideline, based on experience, for a good balance

between ROM accuracy and ROM creation duration. However, for a lower number of continuous input factors, i.e., five or less, some users have found more success with the total # Training Runs/Category value around 3*2^n, whereas for a higher number of continuous input factors, i.e., 10 or more, some users have found more success with the total # Training Runs/Category value around 0.2*2^n. As a result, 2^n is the recommended place to start, and users can take advantage of the **ROM Improvement** tab to add more training runs as their ROM requires. The training runs that get created are used to train the data-fitting algorithm to achieve the best data-fit. Please refer to your *Veritrek Customer Support Representative* for more detailed discussion or help with your specific ROM creation use case.

The # Validations Runs/Category value is default set, based on experience, but can be altered to a user-defined value. It is important to note that increasing this value may or may not result in a more accurate ROM, but it will take longer to create. The validation runs that get created are used to validate the trained data-fitting algorithm and are then subsequently used to optimize the data-fit based on the validation results.
*** Helpful Tip – It is also important to note that the minimum required value for the # Validation Runs/Category value is determined by the number of continuous input factors. If you have five continuous input factors, be sure to enter in a value of at least 5 for the # Validation Runs/Category. If a lower value is used, a pop-up will appear giving information on the minimum value that needs to be entered. If this occurs, click OK to exit the pop-up, press the Clear Runs button to clear the runs that were created, enter in an appropriate value for # Validation Runs/Category, and click the Create Runs button again.*

The default sampling algorithm is a LoadPath-developed Latin Hypercube Sampling Algorithm and requires a minimum of four runs per category. Sampling algorithm options can be invoked by clicking on the gear icon next to the chosen sampling algorithm. For the Latin Hypercube Sampling Algorithm, the only option available is a duplication factor value. This value represents the number of times the sampling algorithm is run, with the best sample being used. It is important to note that the LoadPath-developed Latin Hypercube Sampling Algorithm starts off at a random point by nature. Therefore, each time the sampling algorithm is run, different sampling points may be generated even if it is for the exact same run.

Veritrek's data-fitting algorithm is based on collected training data and a lengthscale (l) model parameter. Lengthscale (l) controls the smoothness of the function. Lower values make functions more flexible (Figure 3-18a), while higher values lead to smoother functions and therefore to coarser approximations of the training data (Figure 3-18b). *Veritrek*'s data-fitting algorithm automatically optimizes the model parameters for users. However, *Veritrek* provides users with options for setting the range of lengthscales, and number of steps within the range of lengthscales, to evaluate. In situations where a ROM's data fit is not accurate enough with the default values, a user can adjust the values for the lengthscale range and number of steps to produce a better data-fit.



a **b**

Figure 3-18: Impact of lengthscale (l) model parameter

Testing was performed to try and determine the best default lengthscales and number of steps to use. First, the range of lengthscales was varied during ROM creation and the average mean of the residual and average standard deviation of the residual for the resultant ROMs were used as a metric of comparison. Results can be seen in Figure 3-19.

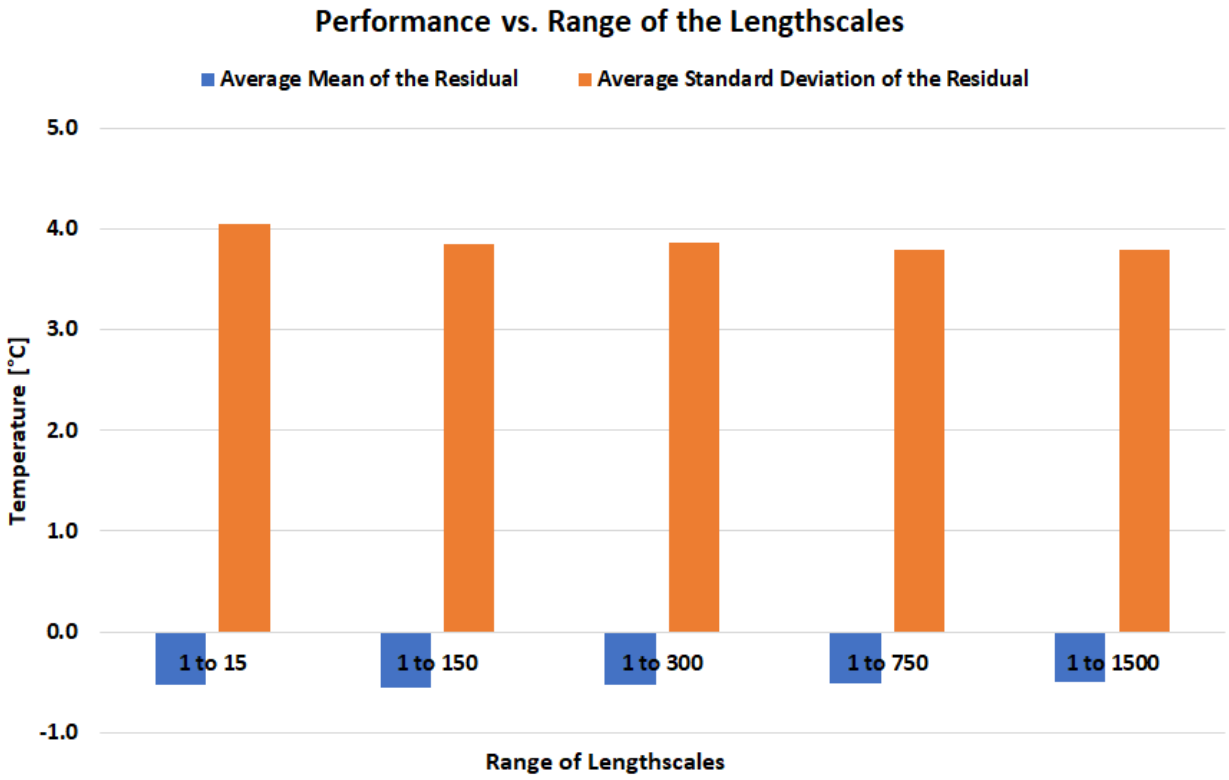


Figure 3-19: Performance vs. Range of Lengthscales

These results show that varying the range of lengthscales does not have a critical impact on the performance of a ROM. Considering the amount of time it took the testing ROMs to get created, a default range of lengthscales from 1 to 100 was chosen. This resulted in good ROM performance without wasting time.

Similar tests were performed by varying only the number of steps between a fixed range of lengthscales, to determine the best default number of steps value to use. Again, the average mean of the residual and average standard deviation of the residual for the resultant ROMs were used as a metric of comparison. Results can be seen in Figure 3-20.

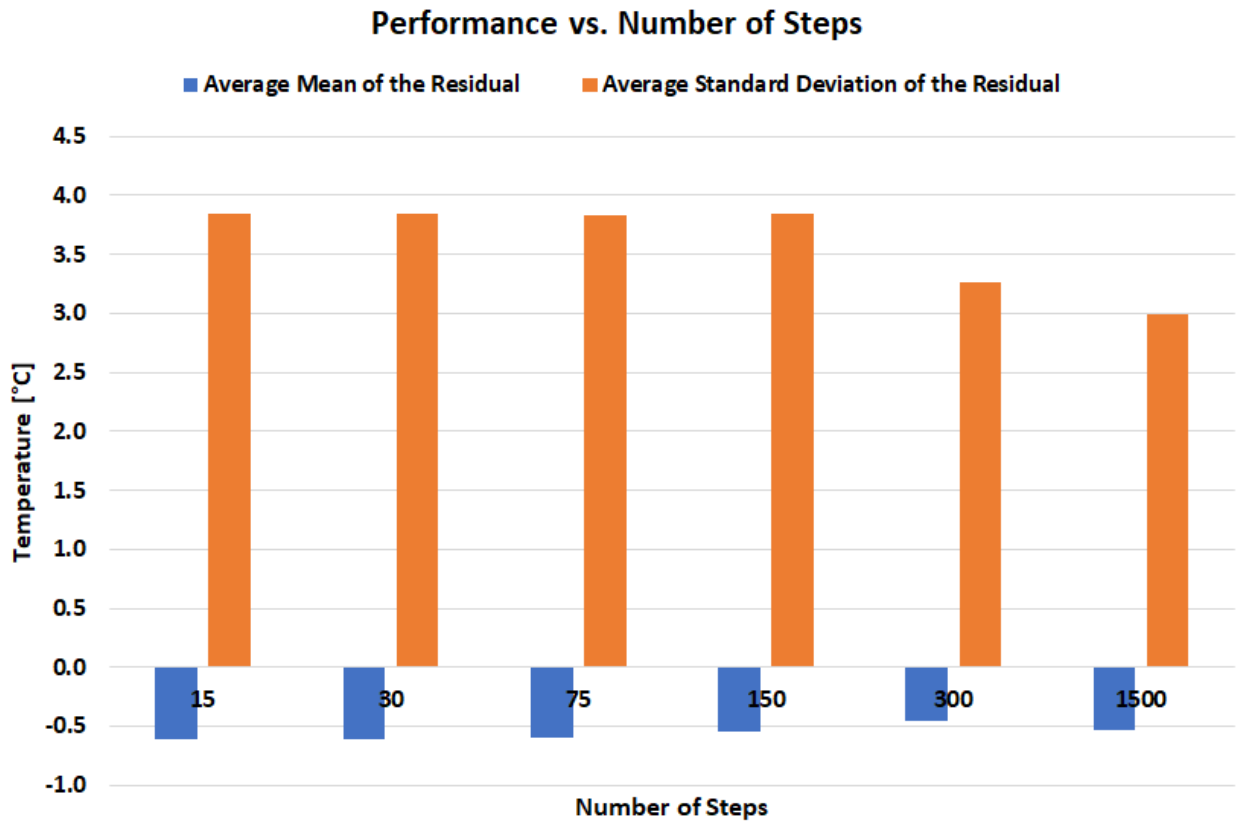


Figure 3-20: Performance vs. Number of Steps

These results show that varying the number of steps does have an impact on the performance of a ROM and seems to bear more importance than the range of lengthscales. Since it took 5x longer to perform the data-fitting with 1500 steps as opposed to 300, the 300 steps shown in Figure 3-20 proved to be the most efficient and represented a value twice that of the maximum lengthscale. Therefore, it was determined to set the default number of steps value to 200 steps since the range of lengthscales has been set to go from 1 to 100.

Data-fitting of register output responses is more nuanced as the quantitative value of a register can vary much more widely than temperature. Registers can be on the order of 10^-6 up to 10^6 or greater. As

such, the data-fitting parameters of lengthscale and steps may need to be adjusted more often when including register output responses in a ROM. Please refer to your *Veritrek Customer Support Representative* for more detailed discussion or help with your specific ROM creation use case.

3.5.3 Clear Runs and Create Runs

After defining the ROM Setup items, the Thermal Desktop® runs can be created by pressing the *Create Runs* button. At this point, the *Veritrek Creation Tool* invokes the chosen sampling algorithm to generate the input factor combinations that will most effectively sample the total design space based on the user-defined parameters. Once runs have been created, they can be cleared using the *Clear Runs* button, in case a user desires to use a different set of runs.

After the runs are created, a pop-up is shown to describe the total number of runs that were created by the *Veritrek Creation Tool*. At this point, the **ROM Creation Status** tab becomes activated.

3.5.4 Import Runs

The user is also given the option to import an existing set of sampling points. Using this option can prove very useful if the user wants to create an identical ROM using the sampling points that were used in the ROM creation of another ROM. Simply click the *Import Runs* button and select a .csv file with the desired sampling runs, and the *Veritrek Creation Tool* will proceed forward with the ROM Creation step with the imported sampling and validation runs.

3.5.5 Divide and Merge Runs

The user is also given the option to divide runs into multiple .lpxml files, or merge together multiple .lpxml files into a single .lpxml files. Users can select the *Divide Runs* button where they will be prompted to identify a number of .lpxml files that they would like to divide the training runs into, as shown in Figure 3-21. After inputting a number and clicking *Divide Runs*, *Veritrek* will save off multiple .lpxml files for the user to load and run.

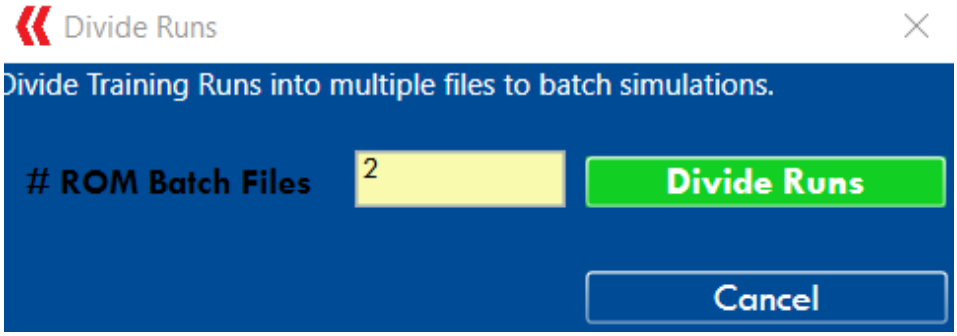


Figure 3-21: Divide Runs

User can also select the *Merge Runs* button to merge multiple .lpxml files back together before performing a data-fit on the combined training data. Veritrek will prompt a user to select the multiple .lpxml files that should be brought back together, and then provide a summary of the number of training data runs, validation runs, and testing runs that were combined. Users can also merge ROMs with different input factor ranges, using this feature, as long as the input factors and output responses remain the same.

3.5.6 ROM Summary

The *ROM Summary* section summarizes the input factors, case sets, and output responses defined in the previous tabs. It is important to note that case sets are treated as another categorical input factor during ROM Creation. This section can be used as a final check to make sure the ROM is set up as desired, before proceeding on to the next step where the ROM gets created.

3.6 ROM Creation Status

Once the **ROM Creation Status** tab becomes activated, it can be selected and will look like Figure 3-22. This tab provides the ability to start and stop the TD runs defined by the sampling algorithm and gives a summary of the ROM creation progress.

There is also the option for the user to export the sampling and validation runs that will be used, which can be useful if the user wants the ability to access these sampling points later and perhaps use them in the future creation of another ROM. Simply click the *Export* button, and the sampling and validation runs will be saved to a .csv file.

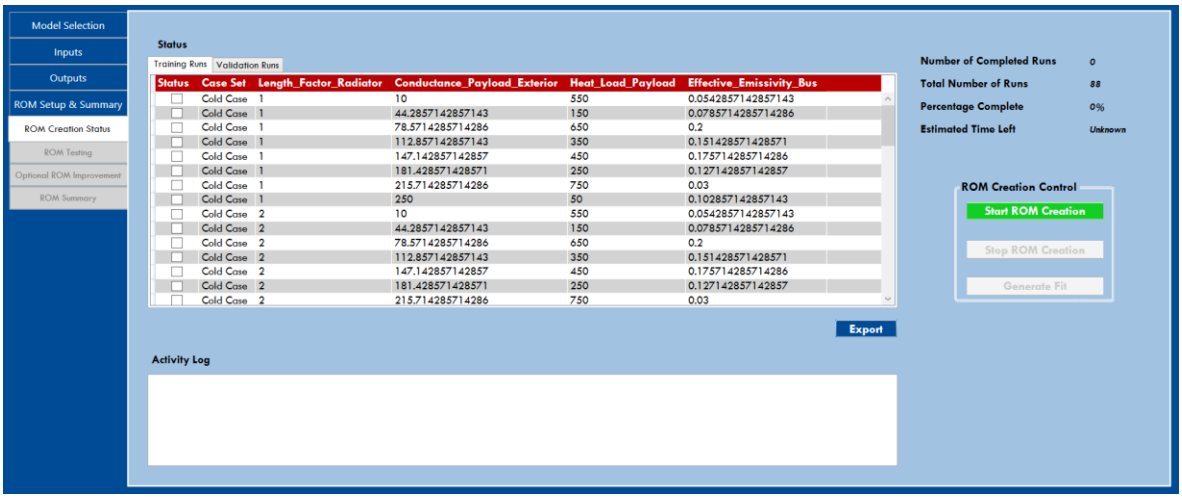


Figure 3-22: The ROM Creation Status tab

The buttons in this frame control the processing of the high-fidelity TD runs that form the inputs to the ROM data-fitter. The *ROM Creation Control* section allows the start and stops of ROM creation and activates the *Generate Fit* button once the runs are completed. Before clicking on *Start ROM Creation*, both the *Stop ROM Creation* and *Generate Fit* buttons are desensitized. Once *Start ROM Creation* is selected, the *Veritrek Creation Tool* begins to write information to the *Activity Log* and Thermal Desktop® opens. The *Activity Log* describes how the original TD drawing file is renamed, the status of each run (started, completed, etc.), and when the ROM sampling is complete. After each simulation completes, the "Number of Completed Runs," "Total Number of Runs," "Percentage Complete," and "Estimated Time Left" texts are updated, the "Status" checkbox of the simulation is checked, and the *Veritrek Creation Tool* automatically saves the ROM session file. This process continues until all runs are complete.

While the TD runs are underway, the ROM creation process can be paused by clicking the *Stop ROM Creation* button. A GUI opens confirming the pause of ROM Creation, and then the process will be paused

after Thermal Desktop® completes the run it is currently working on. The ROM session file will still contain all the simulation data previously created, and the *Veritrek Creation Tool* can be exited. In this way, the simulations can be resumed later, by clicking the *Start ROM Creation* button again. However, it is important to note that the next tab will not activate until all the runs are completed. Once the runs are completed, the *Generate Fit* button is activated. When this button is selected, the *Veritrek Creation Tool* performs the fit on the simulation data and then automatically activates and selects the **ROM Testing** tab.

The fit is performed by writing out the four files required by the data-fitting algorithm. The first is the detailed model file, which provides high-level details of a model. The naming convention is "Modelname.dat," where Modelname is the ROM name. The second is the input point's file, which is a tab-delimited array of specific sampling points. The naming convention is "Modelname_Points.dat." The third file is the training data file, which contains a tab-delimited array of output responses. The naming convention is "Modelname_Ytr.dat." The fourth file is the validation data file, which contains a tab-delimited array of output response, with the naming convention of "Modelname_Validation.dat." The *Veritrek Creation Tool* uses these files to generate the fit coefficients and respective coefficients file used by the *Veritrek Exploration Tool*. The fit coefficients file provides the array of specific coefficients and follows the naming convention of "Modelname_Coefficients.dat." Together, the detail file and the coefficients file fully define the ROM.

3.7 ROM Testing

Once the **ROM Testing** tab becomes activated, it can be selected and will look like Figure 3-23. In this tab, the performance of the ROM is compared to that of the original high-fidelity TD model. This involves solving several additional TD runs, computing the estimated results from the ROM using the same inputs, and comparing the outputs of both. When the test simulations are completed, the results for each output response for each TD run and ROM prediction are written to a comma-delimited text file. The naming convention is "Modelname_test.dat." These steps are described in more detail in the following sections.

Figure 3-23: The ROM Testing tab

3.7.1 Testing Setup

The *Testing Setup* section allows a user to define and create the ROM tests. It consists of six options:

1. "Number of Test Runs" – defines how many ROM test run are to be performed, with a minimum of four test runs required
2. "Test Sampling Options" – selects the method to create the test runs
3. *Create Test Runs* – creates the ROM tests runs once (1) and (2) are set
4. *Clear Test Runs* – clears the ROM test runs
5. *Import Test Runs* – imports already created test runs from a saved .csv file
6. *Export Test Runs* – exports the currently created test runs and saves them to a .csv file

Once the *Create Test Runs* button is selected, the program creates the test runs that will be performed using Thermal Desktop® and computes the estimated ROM values for the associated test runs. The runs appear in the *ROM Testing Status* section, and the *Start ROM Testing* button in the *ROM Testing Control* subsection becomes active.

3.7.2 ROM Testing Control

The *ROM Testing Control* section allows a user to begin or stop the ROM testing. After creating the test runs, only the *Start ROM Testing* button is active. Once this box is selected, the *Stop ROM Testing* button becomes available.

3.7.3 ROM Testing Status

The *ROM Testing Status* section provides a table of the ROM test runs to be analyzed. Each row consists of a unique test run; the columns consist of the status, case set, and inputs analyzed. Before the *Start ROM Testing* button is selected, the table is desensitized, but once it is selected, the entire table becomes active.

3.7.4 Outputs

The *Outputs* section allows a user to plot any output response after the ROM testing is complete, to observe how the ROM is performing relative to the underlying Thermal Desktop® model for that output response. It lists the output response name and output type (minimum/mean/maximum temperature/incident heat/register). Output responses can then be selected and plotted using the *Plot Outputs* button. Alternatively, the output response can be double-clicked. The *Veritrek Creation Tool* will then plot the selected outputs. An example is shown in Figure 3-24.

Each plot displays the ROM prediction versus the measured TD result for that output response. The horizontal axis represents the measurement obtained from the underlying Thermal Desktop® model, and the vertical axis represents the prediction by the ROM. The green dashed line represents a perfect correlation between the ROM and the high-fidelity TD model. The red circles are the test run points. The closer the red circles are to the green line, the more accurate the ROM is. Data points can be hovered over until an upward-facing arrow appears. When the circle is clicked, the value of the data point will appear on the screen.

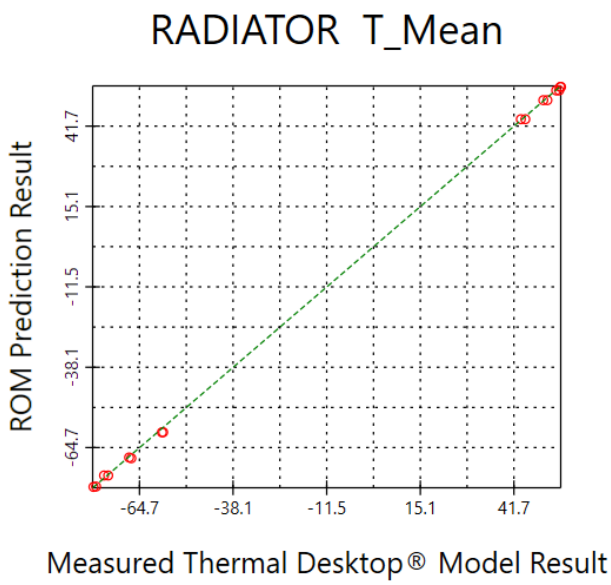


Figure 3-24: Example plot output GUI

3.7.5 Activity Log

The *Activity Log* section lists the progress of the ROM testing. It describes the status of each run (started, completed, etc.), and when the ROM testing is complete.

3.8 Optional ROM Improvement

Once the **Optional ROM Improvement** tab becomes activated, it can be selected and will look like Figure 3-23. This is an optional step in the ROM creation process. If a ROM is created and test results from the **ROM Testing** tab show that the created ROM is not accurate enough for its intended rapid thermal analysis application, this tab allows a user to add additional sampling points to the already-created ROM. The functions of this tab work the same as those in the previous **ROM Setup & Summary** tab, **ROM Creation Status** tab, and **ROM Testing** tab.

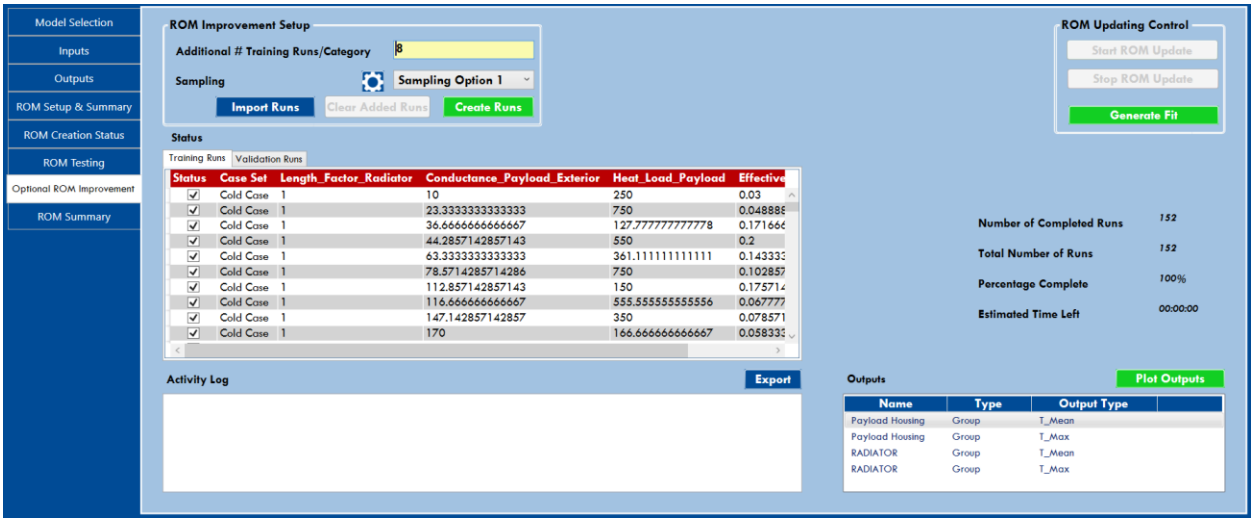


Figure 3-25: The Optional ROM Improvement tab

3.8.1 ROM Improvement Setup

The *ROM Improvement Setup* section allows a user to add additional training runs to an already-created ROM. It consists of five options:

1. "Additional # Training Runs/Category" – defines how many additional trainings per category a user would like to add to their ROM
2. "Sampling" – selects the method to create the additional training runs
3. *Create Runs* – creates the additional training runs
4. *Clear Added Runs* – clears the additional training runs
5. *Import Runs* – imports additional runs from a .csv file

Once the *Create Runs* button is selected, the program creates the additional training runs that will be performed using Thermal Desktop® and adds them into the *Status* table. The *Create Runs* button in the *ROM Updating Control* subsection becomes active.

*** Helpful Tip – After clicking the Create Runs or Import Runs button, a pop-up will appear warning you that updating the ROM will result in overwriting the already-existing data. You will be given the option to overwrite the data with the same ROM name information, or rename the ROM so that you can have access to the previous ROM iteration and the updated ROM. You can also choose to remove this pop-up from appearing in the future. If you do remove this pop-up in the future, you can have it show up again if you go to Help>Restore Default Settings.*

3.8.2 ROM Updating Control

The *ROM Updating Control* section allows a user to start or stop the ROM update. After creating additional training runs only the *Start ROM Update* button is active. Once this box is selected, the *Stop ROM Update* button becomes available. After the additional training runs are performed in Thermal Desktop®, the *Generate Fit* button becomes available and should be selected to complete the creation of the updated ROM. Once *Start ROM Update* is selected, the *Veritrek Creation Tool* begins to write information to the *Activity Log* and Thermal Desktop® opens. The *Activity Log* describes how the original TD drawing file is renamed, the status of each run (started, completed, etc.), and when the ROM sampling is complete. After each simulation completes, the "Number of Completed Runs," "Total Number of Runs," "Percentage Complete," and "Estimated Time Left" texts are updated, the "Status" checkbox of the simulation is checked, and the *Veritrek Creation Tool* automatically saves the ROM session file. This process continues until all additional training runs are complete.

3.8.3 Status

The *Status* section provides a table of the ROM Training Runs, and Validation Runs, to be analyzed. Each row consists of a unique training run; the columns consist of the status, case set, and inputs analyzed. Once additional training runs are created, they will appear in the *Training Runs* tab of the *Status* table and their status checkbox will be empty.

3.8.4 Outputs

The *Outputs* section allows a user to plot any output response after the additional training runs are completed and the new data fit is completed. The test runs are still used from before, but the ROM

prediction results are recalculated based on the updated ROM. These test plots work in the exact same way as the do with the **ROM Testing** tab and allow a user to observe how the ROM is performing relative to the underlying Thermal Desktop® model for that output response. It lists the output response name and output type (minimum/mean/maximum temperature/incident heat/register). Output responses can then be selected and plotted using the *Plot Outputs* button. Alternatively, the output response can be double-clicked. The *Veritrek Creation Tool* will then plot the selected outputs.

3.9 ROM Summary

After ROM testing is complete, the **ROM Summary** tab becomes activated, and it can be selected. Figure 3-26 shows an overview of the **ROM Summary** tab. It summarizes the input factors and output responses selected for the ROM creation, as well as how well the ROM compares to the TD model. This information is described in more detail in the following sections.

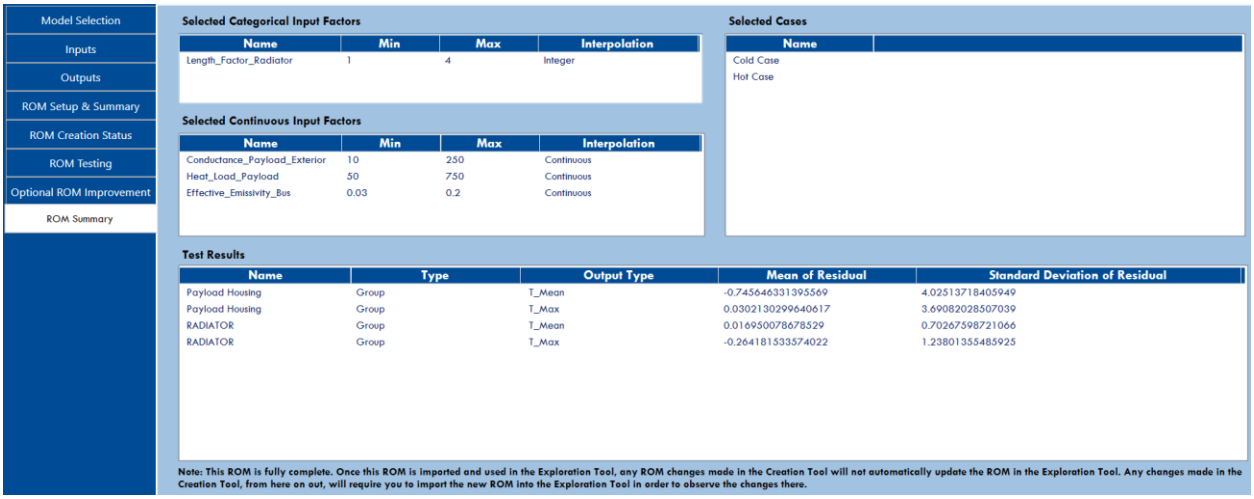


Figure 3-26: The ROM Summary tab

3.9.1 Selected Categorical Input Factors

The *Selected Categorical Input Factors* section summarizes all the categorical input factors selected for the ROM creation. These are the symbols that were defined with the "MinMax" or "Integer" interpolation types. The columns list the name, minimum, maximum, and interpolation method chosen.

3.9.2 Selected Continuous Input Factors

The *Selected Continuous Input Factors* section summarizes all the continuous input factors selected for the ROM creation. These are the symbols that were defined with the "Continuous" interpolation type. The columns list the name, minimum, maximum, and interpolation method chosen.

3.9.3 Selected Cases

The *Selected Cases* section lists the case sets chosen for the ROM creation.

3.9.4 Test Results

The *Test Results* section summarizes all the output responses selected for the ROM creation. The columns include the description of the output responses chosen (name, type, and output type) as well as the

statistical results of the ROM analysis (mean of residual and standard deviation of residual). The statistical results can be reviewed to determine the accuracy of the ROM.

The mean of residual is calculated as the average difference of the ROM from the actual data, whereas the standard deviation of the residual is calculated as the square root of the difference of the mean residual squared from the difference of the ROM from the actual data squared. These calculations can be summarized by the following formulas:

$$meanRes = \frac{\sum_{i=1}^{n}(romResults[i] - actualResults\ [i])}{n}$$

$$stdDev = \sqrt{(romResults[i] - actualResults\ [i])^2 - meanRes^2}$$

4 TUTORIALS

This section of the *Veritrek Creation Tool User's Manual* is intended as a step-by-step walkthrough of the *Veritrek Creation Tool*. There is an example problem, which will be shown along with pictures and click-by-click instructions, on how to work through this application tool. There is one demo model that comes pre-loaded with the tool. The example that will now be shown represents a single use case for the *Veritrek Creation Tool and* is merely provided to demonstrate how to use the tool.

4.1 Communications Satellite Demo Example Problem

4.1.1 Description of the VeritrekCT_demoA Thermal Desktop® Model

The easiest way to learn the basics of the *Veritrek Creation Tool* is to create a ROM using the example model provided. The example model is found in the "demo" folder, located in \Program Files\Veritrek\Creation Tool\demo. It is best to copy this folder to another location before performing the demo.

The model, shown in Figure 4-1, is a generic communications satellite in low Earth orbit. The model includes eight submodels that are broken out into the various components of the satellite, for a total of 181 nodes.

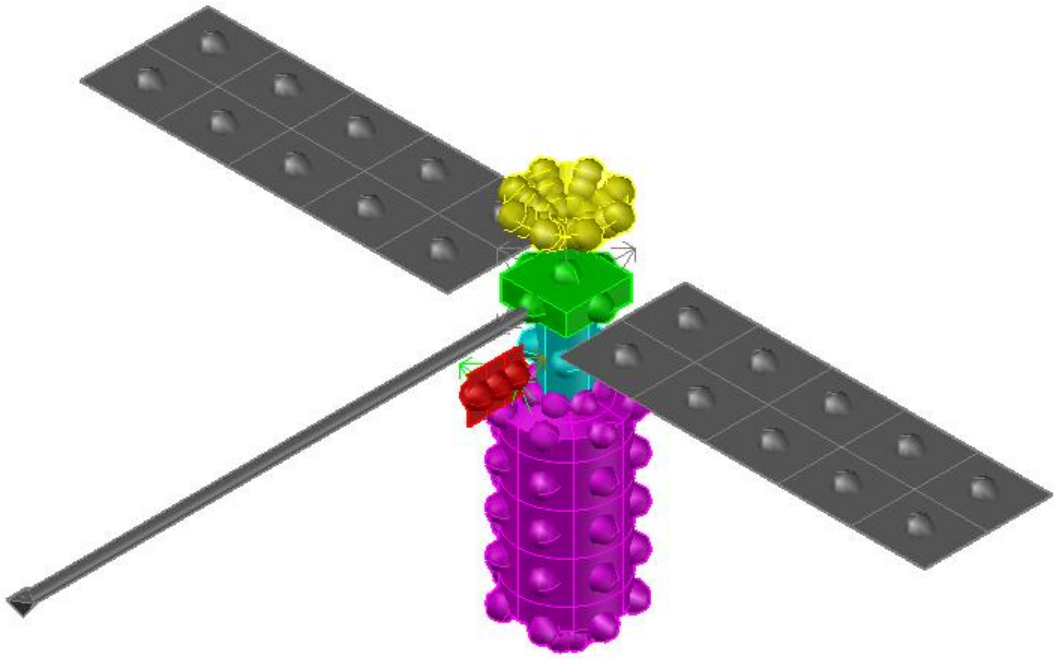


Figure 4-1: VeritrekCT_demoA - Communications Satellite demo model

A breakdown of the nine submodels, and the different Thermal Desktop® objects they include, can be seen in Table 1.

Table 1: Submodels included in VeritrekCT_demoA

Submodel	# of Nodes	# of Conductors	# of Heat Loads	# of Contactors
ANTENNA	24	0	0	0
BOUNDARY	1	1	0	0
BUS	57	0	0	1
BUS_INSULATION	57	0	0	1
PAYLOAD	10	4	1	3
PAYLOAD_INSULATION	10	4	0	3
RADIATOR	3	0	0	1
SOLAR_ARRAY_-Y	10	0	0	0
SOLAR_ARRAY_+Y	10	0	0	0

The four symbol groups of Conductance, Geometry, Heat Load, and Optical will be used in the Tutorial, and can be used to explore some of the capabilities that the *Veritrek Creation Tool* provides in terms of the types of parameters that can be captured and utilized in a ROM. A list of symbols and their descriptions can be seen in Table 2.

Table 2: Symbols included in VeritrekCT_demoA

Symbol Group	Symbol Name	Description
Conductance	Conductance_Payload_Bus_Rad	Total conductance value between the Payload, Bus, and Radiator components [W/K].
	Conductance_Payload_Exterior	Total conductance value from the payload electronics to the external surface of the satellite [W/K].
Geometry	Length_Factor_Radiator	Scaling Factor for the length of the satellite's 4m wide radiator, in increments of 5 m: 1 = 5m, 2 = 10m, 3 = 15m, 4 = 20m.
	Location_Electronics	Mounting location of internal payload electronics: 0 = +Z face, 1 = +X face, 2 = +Y face
Heat Load	Heat_Load_Payload	Heat load applied to the satellite's payload [W].
Optical	Absorptivity_Bus	Absorptivity value for the external surface of the satellite's bus.
	Absorptivity_Radiator	Absorptivity value for the external surface of the satellite's radiator.
	Effective_Emissivity_Bus	Effective emissivity value for the insulation of the satellite's bus.
	Emissivity_Bus	Emissivity value for the external surface of the satellite's bus.
	Emissivity_Radiator	Emissivity value for the external surface of the satellite's radiator.

In addition to the symbols described above, the two case sets used in the tutorial represent a hot case orbit environment and a cold case orbit environment. Details can be seen in Table 3.

Table 3: Case Sets included in VeritrekCT_demoA

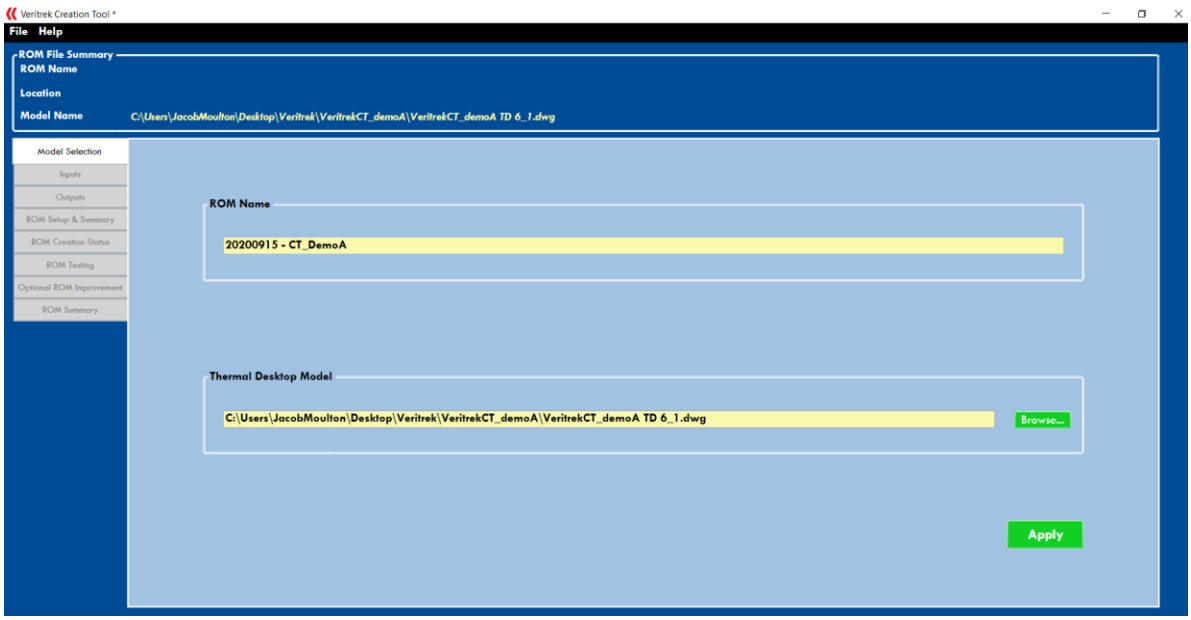
Case Set	Beta Angle	Altitude	Pointing	Solar Flux	Albedo
Cold Case	0°	1000 km	Nadir	1317 W/m^2	0.18
Hot Case	72°	350 km	Nadir	1419 W/m^2	0.392
Variable Environment Case	symbol	symbol	Nadir	symbol	symbol

4.1.2 Preparing the Model for the *Veritrek Creation Tool*

Copy the model files (VeritrekCT_demoA TD 6_1.dwg, VeritrekCT_demoA.rco, and VeritrekCT_demoA.tdp) from the "demo" directory to another directory and open the model file. Verify that the model is working by running the three case sets.

4.1.3 Click-by-click Solution

Model Selection	
Open the tool so that the *Main Window* is visible.	Ensure that the Model Selection tab is selected, and the tool is focused on this tab.
1. *Type* in "DATE – CT_DemoA" for ROM Name.	
2. *Select* the VeritrekCT_demoA TD 6_1.dwg from its user-specified directory**.**	If you are not running TD 6.1 yet, you can use the older .dwg file.



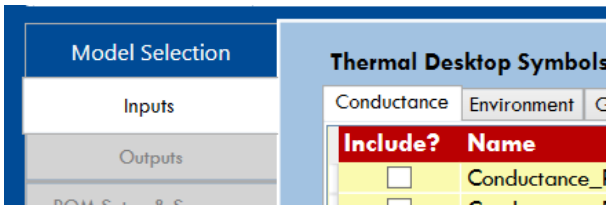
3. *Click* **Apply**.

4. *Select* a location to save the ROM file.

5. *Click* **Save**.

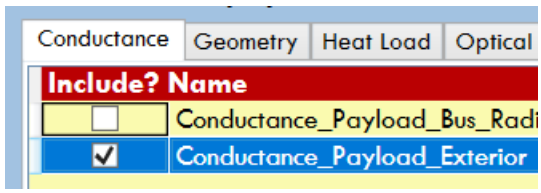
At this point, the *Veritrek Creation Tool* will automatically open the selected .dwg file. After the file successfully opens it will close, and the Inputs and Outputs tabs will become available in the *Veritrek Creation Tool*.

Veritrek will automatically move to the *Inputs* tab.



6. *Select to include* "Conductance_Payload_Exterior" from the Conductance group.

This checkbox is in the "Thermal Desktop® Symbols" section of the *Inputs* tab.



7. *Set* the "Minimum Value' for "Conductance_Payload_Exterior" to **10**, the "Maximum Value" to **250**, and the "Interpolation Method" to **Continuous**.

These options can be set under the "Inputs Summary" section of the *Inputs* tab.

8. *Select to include* "Length_Factor_Radiator" from the Geometry group.

9. *Set* the "Minimum Value' for "Length_Factor_Radiator" to **1**, the "Maximum Value" to **4**, and the "Interpolation Method" to **Integer**.

Inputs

10. *Select to include "*Heat_Load_Payload" from the Heat Load group.

11. *Set* the "Minimum Value' for "Heat_Load_Payload" to **50**, the "Maximum Value" to **750**, and the "Interpolation Method" to **Continuous**.

12. *Select to include "*Effective_Emissivity_Bus" from the Optical group.

13. *Set* the "Minimum Value' for "Effective_Emissivity_Bus" to **0.03**, the "Maximum Value" to **0.2**, and the "Interpolation Method" to **Continuous**.

Inputs Summary

Group	Name	Nominal Value	Minimum	Maximum	Interpolation
Conductance	Conductance_Payload_Exterior	50	10	250	Continuous
Geometry	Length_Factor_Radiator	1	1	4	Integer
Heat Load	Heat_Load_Payload	200	50	750	Continuous
Optical	Effective_Emissivity_Bus	0.03	0.03	0.2	Continuous

Navigate to the bottom of the *Inputs* tab, in the Thermal Desktop Case Sets section.

14. *Select* "Hot case" and *click* **Add**.

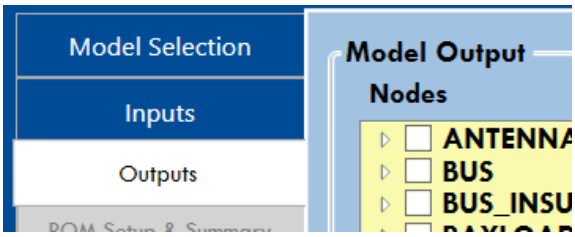
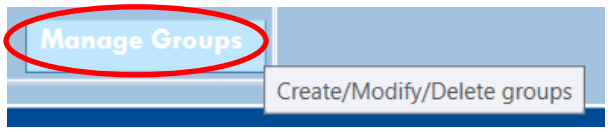
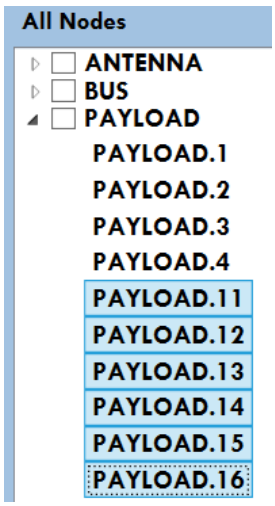
15. *Select* "Cold case" and click **Add**.

16. *Click* **Check Inputs**.

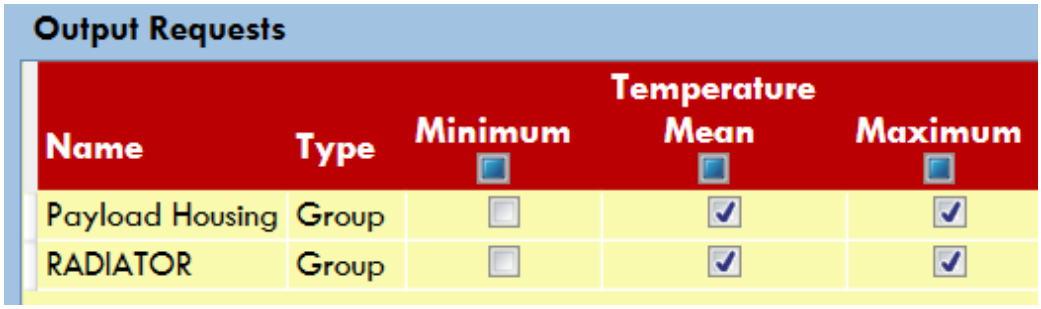
17. *Click* **OK**.

These case-sets can be added under the "Thermal Desktop® Case Sets" section of the *Inputs* tab.

This step verifies that all inputs are correct. If they are not correct, an information box will pop up with the details on what needs to be changed.

Outputs	
Veritrek will automatically move to the *Outputs* tab.  18. *Click* **Manage Groups**.	
 19. *Click* **Create**.	This option is located at the bottom of the pane. These steps are performed to create a group called "Payload_Housing" that will include nodes 11 thru 16 of the Payload submodel.
20. *Type* "Payload Housing" and *Click* **OK**.	
21. *Select* **PAYLOAD** to open up the dropdown menu.	This option is located under the "All Nodes" section of the "Edit Group Nodes" block.
22. *Press and hold* **SHIFT**, *and Click to select* PAYLOAD.11, PAYLOAD.12, PAYLOAD.13, PAYLOAD.14, PAYLOAD.15, and PAYLOAD.16 	The form should look like this image.
23. *Click* **Add**.	
24. *Click* **OK**.	This will exit the form and re-focus to the *Veritrek Creation Tool*.

Outputs	
25. *Select to include* the **Payload Housing** node group. 26. *Select to include* the **RADIATOR** node group. 27. *Select to include* the Mean and Maximum Temperatures for both node groups.	This option is located under the "Output Requests" block of the *Outputs* tab. For simplicity, toggle these options by selecting the box at the top of each column. The *Outputs* tab should look like the image below.



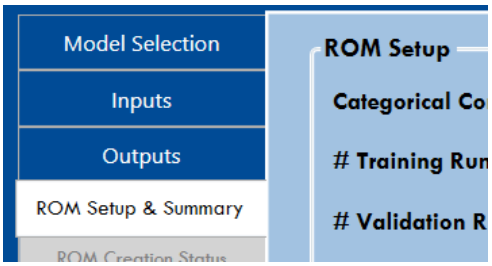
Output Requests

Name	Type	Minimum	Temperature Mean	Maximum
Payload Housing	Group	☐	☑	☑
RADIATOR	Group	☐	☑	☑

28. *Click* **Check Outputs**. 29. *Click* **OK.** 30. *Click* **Yes** to allow *Veritrek* to perform Model Checks. 31. *Click* **OK** to confirm that the model passed the necessary checks.	This step verifies that all outputs are correct. If they are not correct, an information box will pop up with the details on what needs to be changed. At this point, the *Veritrek Creation Tool* will ask to check model which is required to continue. The *Veritrek Creation Tool* will once again open up and close the selected .dwg file, and notify of a successful model check.

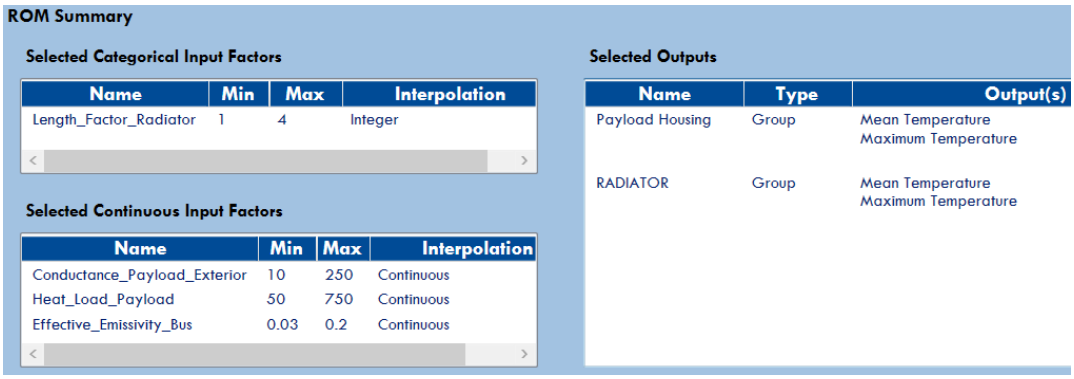
ROM Setup & Summary

Veritrek will automatically move to *the ROM Setup & Summary* tab.



32. Leave the # Training Runs/Category at **8**.

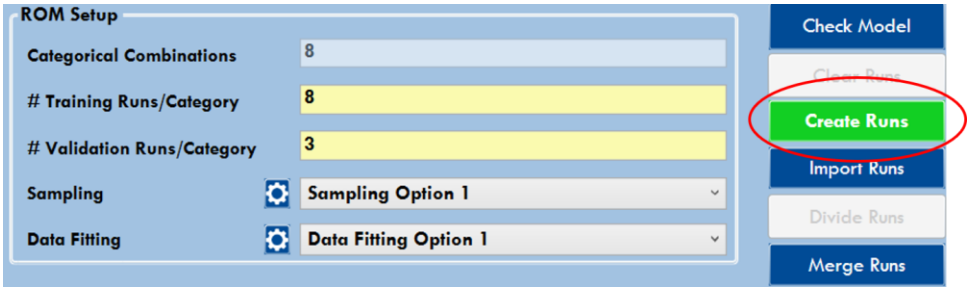
33. Verify that the ROM Summary information matches the image below, and that both Cold Case and Hot Case show up in the Selected Case Sets section.



34. *Click* **Create Runs**.

35. *Click* **OK** to confirm number of runs created.

The *Veritrek Creation Tool* will automatically move to the *ROM Creation Status* tab after creating the runs.

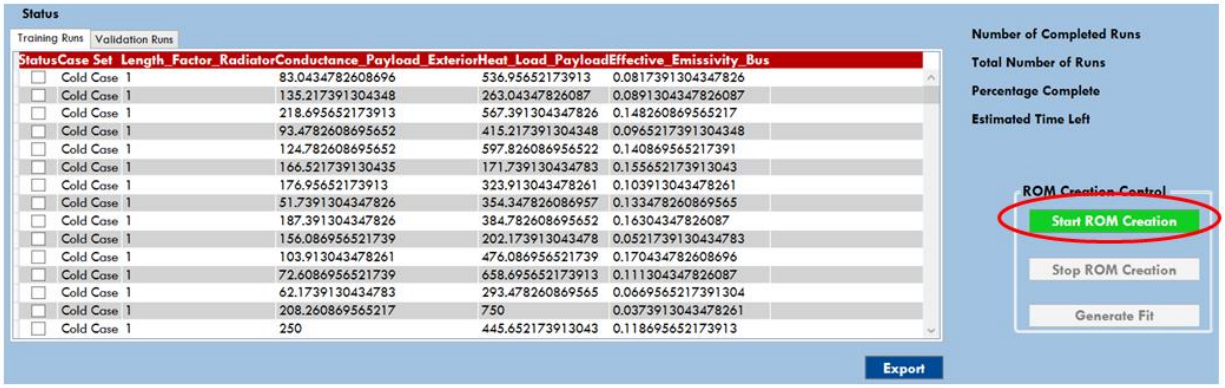


ROM Creation Status

Veritrek will automatically move to the *ROM Creation Status* tab.

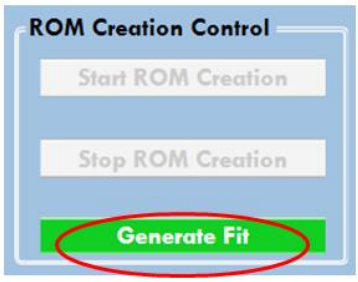
36. *Click* **Start ROM Creation**.

The model will now run for about 30 to 60 minutes, depending on the speed of the computer performing the calculations. After each run is completed, the *Veritrek Creation Tool* will automatically save the file. If the calculations need to be stopped for any reason, simply click the **Stop ROM Creation** button to stop the current simulation. The **Start ROM Creation** button can then be clicked to resume the calculations. Once complete, proceed to the next step.



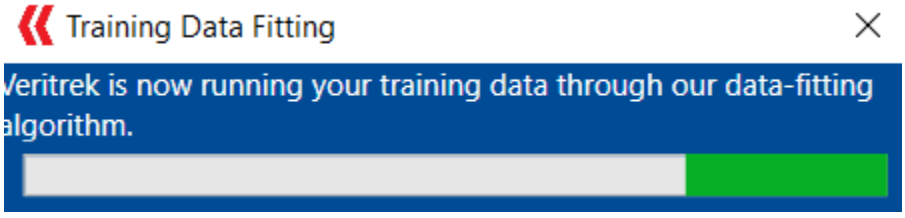
Veritrek will automatically unlock the "Generate Fit" button.

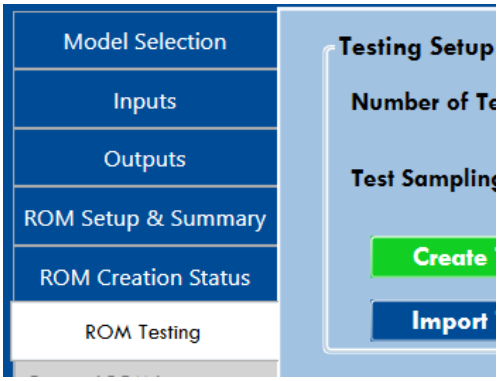
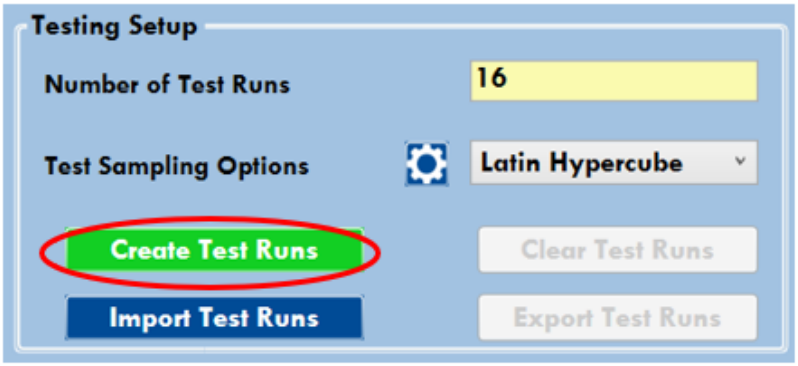
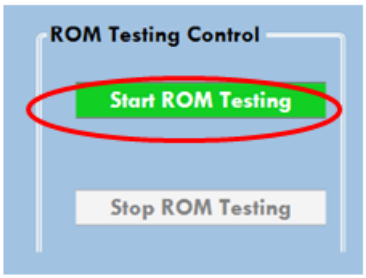
37. *Click* the **Generate Fit** button.



Veritrek will now solve for about 15 minutes. This will create the ROM files.

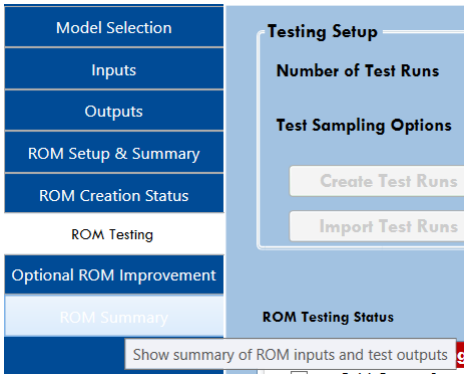
Once complete, the ROM is fully created. The next steps consist of testing and verifying the accuracy of the ROM.



ROM Testing	
Veritrek will automatically move to the *ROM Testing* tab.  38. *Click* the **Create Test Runs** button.	For this tutorial example, the defaults selected are sufficient for ROM Testing.
 	
39. *Click* the **Start ROM Testing** button.  	The model will now run for about 10 to 20 minutes, depending on the speed of the computer performing the calculations. After each run is completed, the *Veritrek Creation Tool* will automatically save the file. If the calculations need to be stopped for any reason, simply click the **Stop ROM Creation** button to stop the current simulation. The **Start ROM Creation** button can then be clicked to resume the calculations. Once complete, proceed to the next step.

ROM Summary

40. *Select* the *ROM Summary* tab.



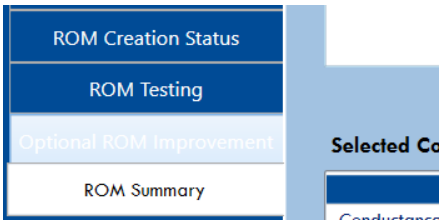
41. Observe similar results to those shown below.

This is where the user must make the judgement call on if the ROM is accurate enough for its intended rapid thermal analysis application.

Test Results

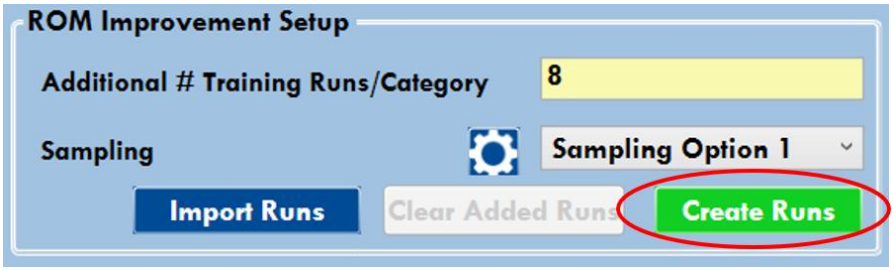
Name	Type	Output Type	Mean of Residual	Standard Deviation of Residual
Payload Housing	Group	Mean Temperature	-0.544779598450889	4.43507517198111
Payload Housing	Group	Maximum Temperature	0.099301275718644	5.51939632243224
RADIATOR	Group	Mean Temperature	-0.0638468557481691	0.934446620807729
RADIATOR	Group	Maximum Temperature	0.581705197456948	1.29321961664345

42. *Select* the *Optional ROM Improvement* tab.

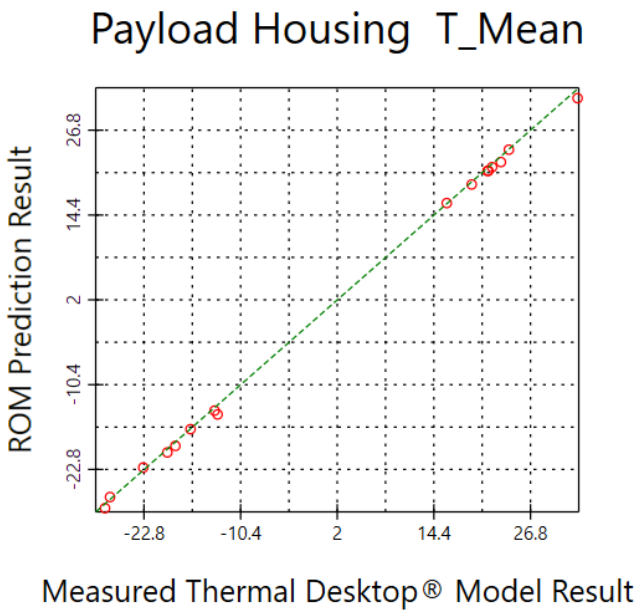


43. Leave the Additional # Training Runs/Category value at 8.

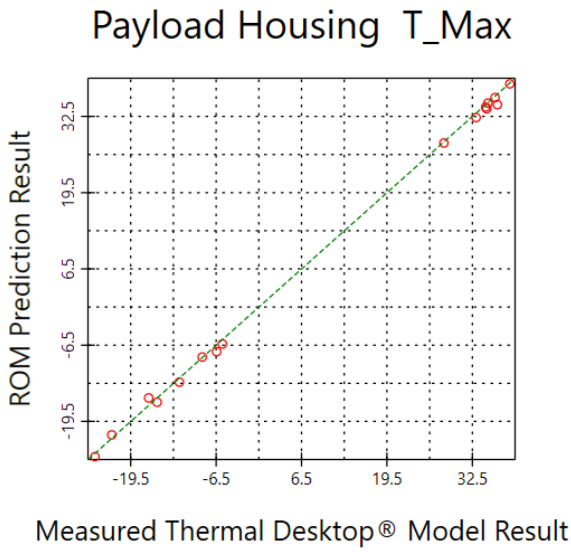
44. *Click* the **Create Runs** button.



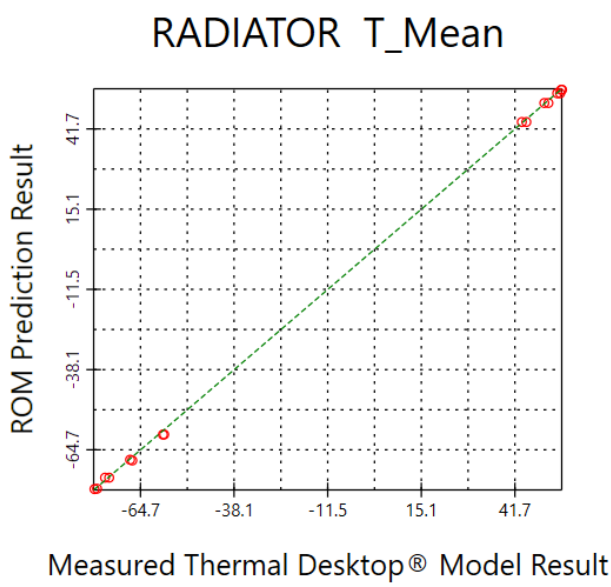
Optional ROM Improvement	
45. *Click* the **Start ROM Update** button. 	The model will now run for about 30 to 60 minutes, depending on the speed of the computer performing the calculations. After each run is completed, the *Veritrek Creation Tool* will automatically save the file. If the calculations need to be stopped for any reason, simply click the **Stop ROM Creation** button to stop the current simulation. The **Start ROM Creation** button can then be clicked to resume the calculations. Once complete, proceed to the next step.
46. *Click* the **Generate Fit** button. 	*Veritrek* will now solve for about 25 minutes. This will create the ROM files.
47. Click the **Plot Outputs** button.	Observe similar results to those shown below.



ROM Testing	
48. Select the *Maximum Temperature* output response for the Payload Housing node group. 49. Click the **Plot Outputs** button.	Observe similar results to those shown below.



50. Select the *Mean Temperature* output response for the RADIATOR node group. 51. Click the **Plot Outputs** button.	Observe similar results to those shown below.

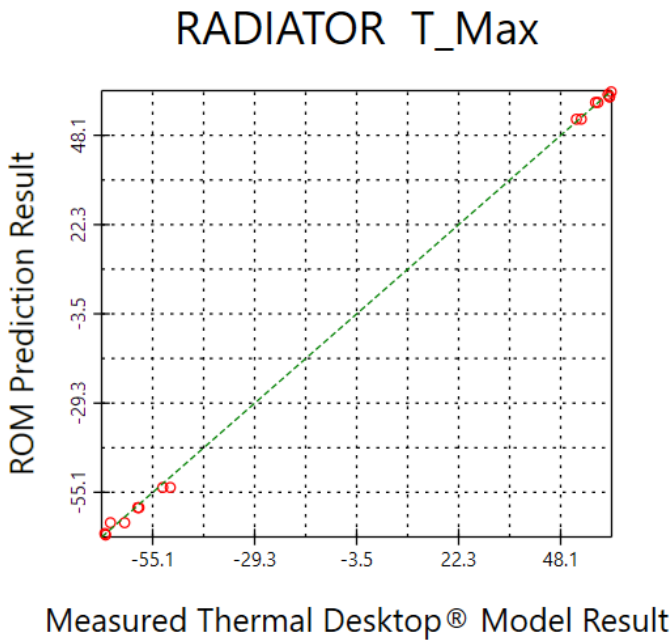


ROM Summary

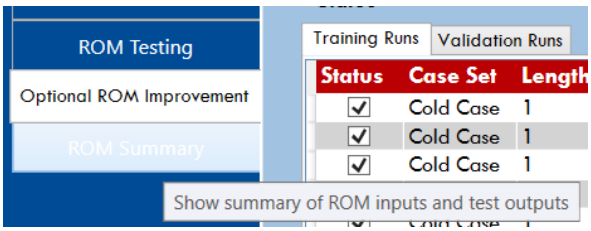
52. Select the *Maximum Temperature* output response for the RADIATOR node group.

53. Click the **Plot Outputs** button.

Observe similar results to those shown below.



54. *Select* the *ROM Summary* tab.



55. Observe similar results to those shown below.

Test Results

Name	Type	Output Type	Mean of Residual	Standard Deviation of Residual
Payload Housing	Group	Mean Temperature	0.274631499533828	1.73711327377232
Payload Housing	Group	Maximum Temperature	-0.0699135720702295	0.373829493054884
RADIATOR	Group	Mean Temperature	-0.065257535678362	0.755962981844312
RADIATOR	Group	Maximum Temperature	0.695702885883005	0.996728149148203

4.2 3U CubeSat Demo Example Problem

4.2.1 Description of the VeritrekCT_demoB Thermal Desktop® Model

The easiest way to learn the basics of the *Veritrek Creation Tool* is to create a ROM using the example model provided. The example model is found in the "demo" folder, located in \Program Files\Veritrek\Creation Tool\demo. It is best to copy this folder to another location before performing the demo.

The model, shown in Figure 4-2 is a generic 3U CubeSat. The model includes ten isothermal PCB components, an isothermal payload component, and an isothermal body-mounted radiator. The CubeSat structure is higher fidelity, along with the body-mounted solar panels. In total this Thermal Desktop® model contains 3183 nodes.

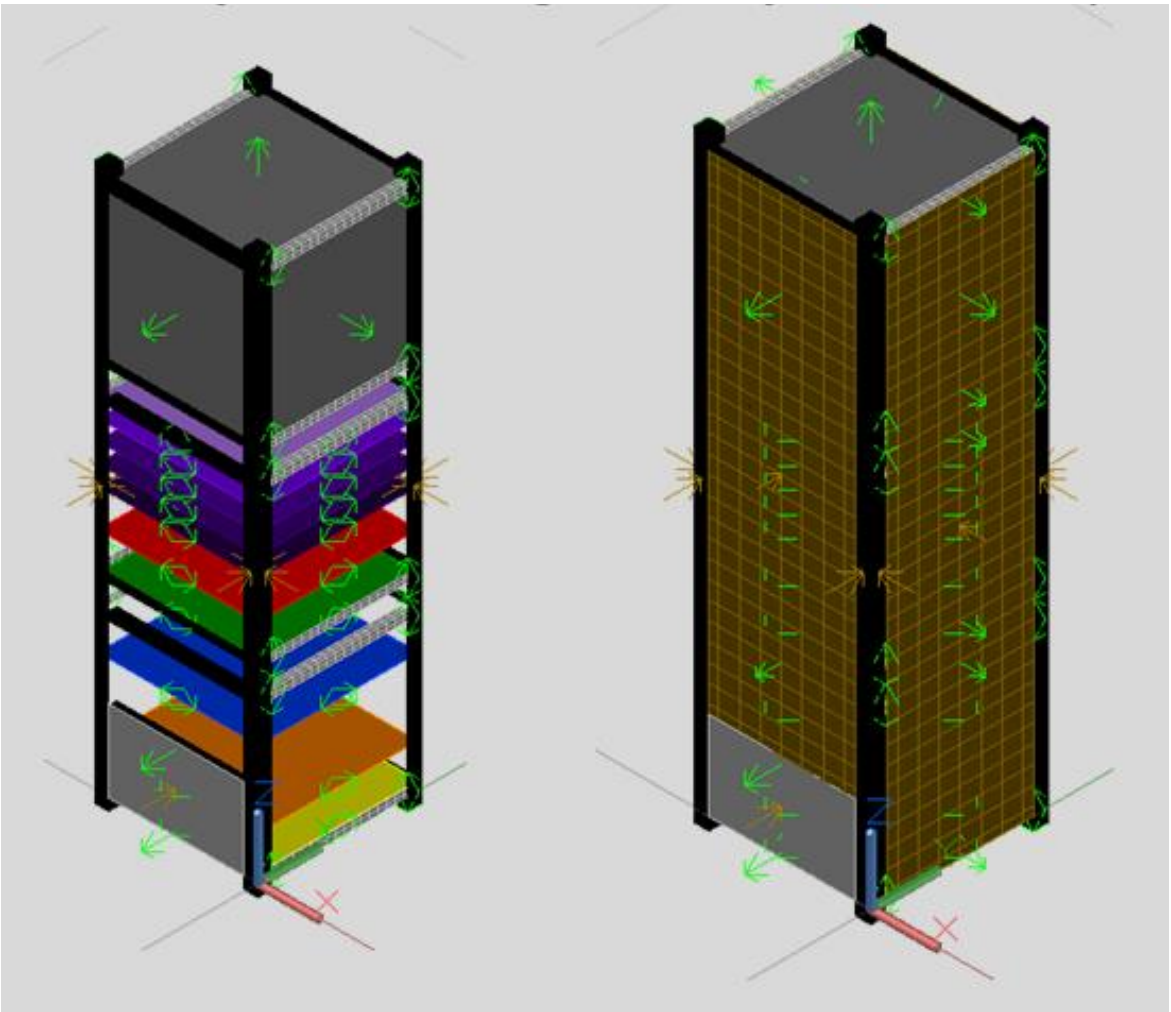


Figure 4-2: VeritrekCT_demoB – 3U CubeSat demo model

A breakdown of the fifteen submodels, and the different Thermal Desktop® objects they include, can be seen in Table 1.

Table 4: Submodels included in VeritrekCT_demoB

Submodel	# of Nodes	# of Conductors	# of Heat Loads	# of Contactors
PAYLOAD	1	0	1	1
PCB0	2	0	1	5
PCB1	2	0	1	5
PCB2	2	0	1	5
PCB3	2	0	1	5
PCB4	2	0	1	5
PCB5	2	0	1	5
PCB6	2	0	1	5
PCB7	2	0	1	5
PCB8	2	0	1	5
PCB9	2	0	1	5
RADIATOR	1	0	0	2
SOLAR_PANEL	1116	0	0	27
STRUCTURE_RAIL_PRIMARY	1433	0	0	80
STRUCTURE_RAIL_SECONDARY	612	0	0	38

The symbol group of "ROM input factors" will be used in the Tutorial, and can be used to explore some of the capabilities that the *Veritrek Creation Tool* provides in terms of the types of parameters that can be captured and utilized in a ROM. A list of the symbols in this group, and their descriptions, can be seen in Table 2.

Table 5: Symbols included in VeritrekCT_demoB

Symbol Name	Description
INPUT_BETA_ANGLE	Beta angle of the satellite's orbit.
INPUT_COMP_CON	Conductance value of the contactor between one corner of the PCM components and the structure rails [W/K].
INPUT_COMP_HF	Heat flux value of the PCM components [W/cm^2].
INPUT_COMP_IPCON	Conductance value of the PCMs in the in-plane direction [W/m-K].
INPUT_COMP_PWR	Power value for the PCM components [W].
INPUT_PAY_PWR	Power value of the Payload component [W].
INPUT_RAD_E	Emissivity of the body-mounted radiator.

In addition to the symbols described above, one case set is set-up to represent an orbit environment. Details can be seen in Table 3.

Table 6: Case Set included in VeritrekCT_demoB

Case Set	Beta Angle	Altitude	Pointing	Solar Flux	Albedo
Orbit	symbol	500 km	Nadir	1354 W/m^2	0.35

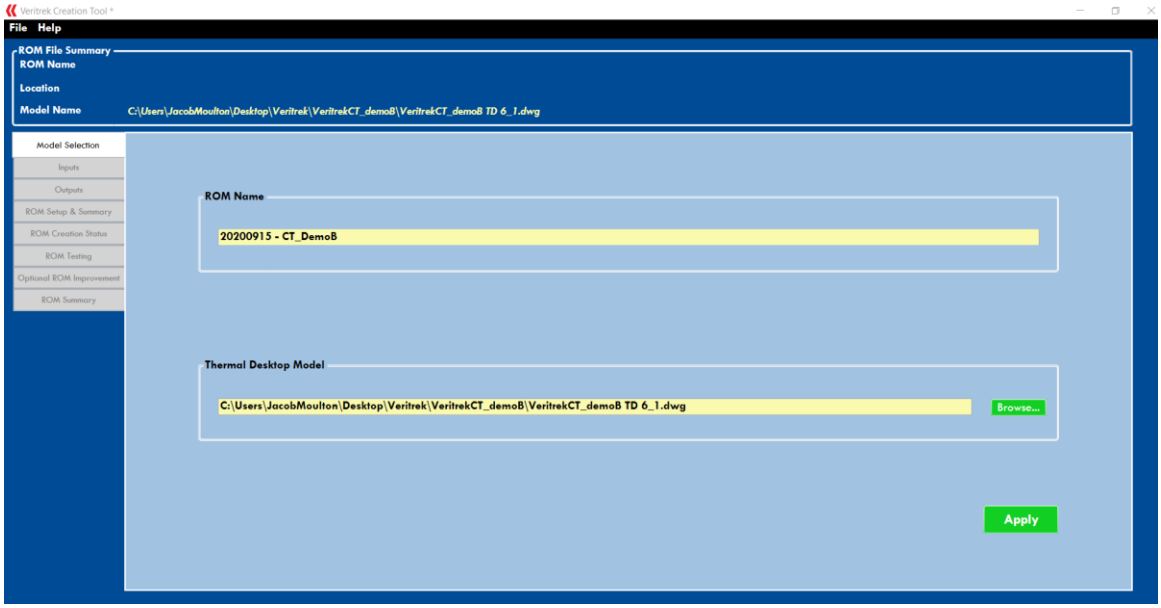
4.2.2 Preparing the Model for the *Veritrek Creation Tool*

Copy the model files (VeritrekCT_demoB TD 6_1.dwg, VeritrekCT_demoB.rco, and VeritrekCT_demoB.tdp) from the "demo" directory to another directory and open the model file. Verify that the model is working by running the one case set.

4.2.3 Click-by-click Solution

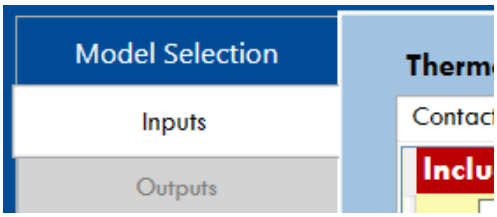
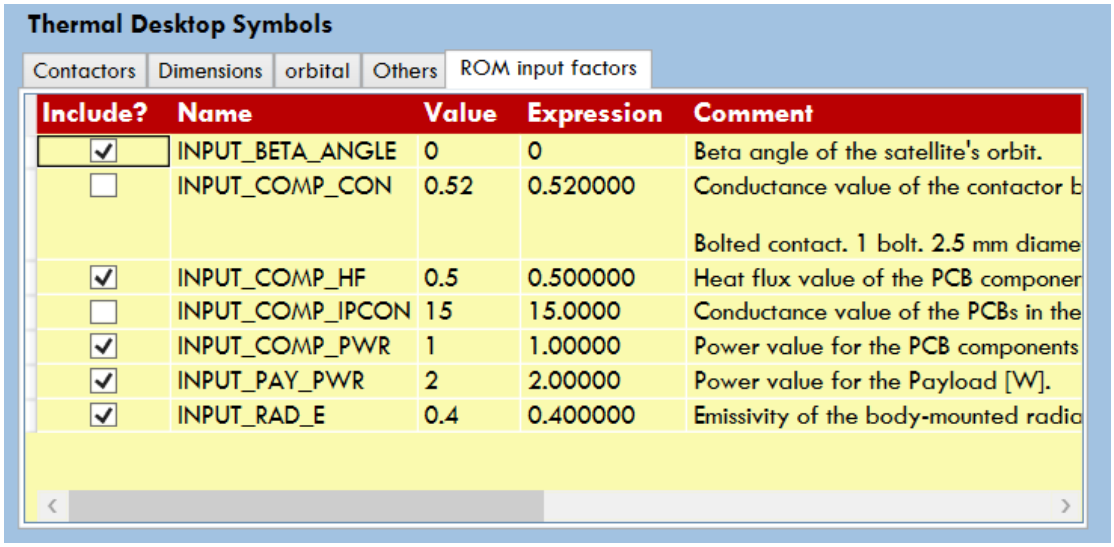
<table>
<tr><th colspan="2">Model Selection</th></tr>
<tr><td>Open the tool so that the Main Window is visible.

1. Type in "DATE – CT_DemoB" for ROM Name.

2. Select the VeritrekCT_demoB TD 6_1.dwg from its user-specified directory.</td><td>Ensure that the Model Selection tab is selected, and the tool is focused on this tab.</td></tr>
<tr><td colspan="2"> 
</td></tr>
<tr><td>3. Click Apply.

4. Select a location to save the ROM file.

5. Click Save.</td><td>At this point, the Veritrek Creation Tool will automatically open the selected .dwg file. After the file successfully opens it will close, and the Inputs and Outputs tabs will become available in the Veritrek Creation Tool.</td></tr>
</table>

Inputs	
Veritrek will automatically move to the *Inputs* tab.  	
6. *Select to include* "INPUT_BETA_ANGLE", "INPUT_COMP_HF", "INPUT_COMP_PWR", "INPUT_PAY_PWR", and "INPUT_RAD_E" from the ROM input factors group.	These checkboxes are in the "Thermal Desktop® Symbols" section of the *Inputs* tab.
 	
7. *Set* the "Minimum Value" for "INPUT_BETA_ANGLE" to **0**, the "Maximum Value" to **90**, and the "Interpolation Method" to **MinMax**. 8. *Set* the "Minimum Value" for "INPUT_COMP_HF" to **0.25**, the "Maximum Value" to **5**, and the "Interpolation Method" to **Continuous**.	

Inputs	
9. *Set* the "Minimum Value" for "INPUT_COMP_PWR" to **0.5**, the "Maximum Value" to **5**, and the "Interpolation Method" to **Continuous**. 10. *Set* the "Minimum Value" for "INPUT_PAY_PWR" to **0.5**, the "Maximum Value" to **10**, and the "Interpolation Method" to **Continuous**. 11. *Set* the "Minimum Value" for "INPUT_RAD_E" to **0.5**, the "Maximum Value" to **0.9**, and the "Interpolation Method" to **Continuous**.	

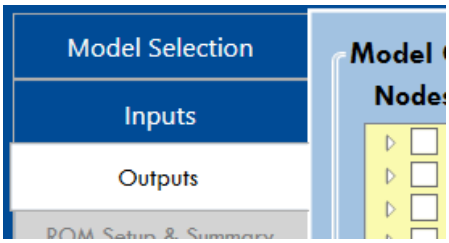
Inputs Summary

Group	Name	Nominal	Minimum	Maximum	Interpolation Metho
ROM input	INPUT_BETA_ANGLE	0	0	90	MinMax
ROM input	INPUT_COMP_HF	0.5	0.25	5	Continuous
ROM input	INPUT_COMP_PWR	1	0.5	5	Continuous
ROM input	INPUT_PAY_PWR	2	0.5	10	Continuous
ROM input	INPUT_RAD_E	0.4	0.5	0.9	Continuous

Navigate to the bottom of the *Inputs* tab, in the Thermal Desktop Case Sets section. 12. *Select* "Orbit" and *click* **Add**. 13. *Click* **Check Inputs**. 14. *Click* **OK**.	This step verifies that all inputs are correct. If they are not correct, an information box will pop up with the details on what needs to be changed.

Outputs

Veritrek will automatically move to the *Outputs* tab.



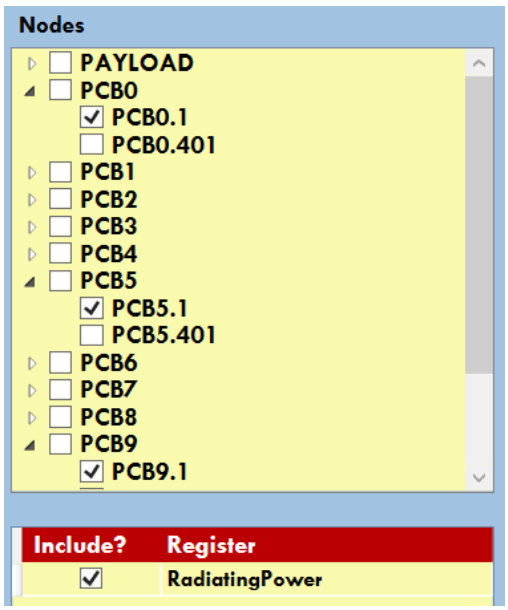
15. *Select to include* the **PCB0.1** node.

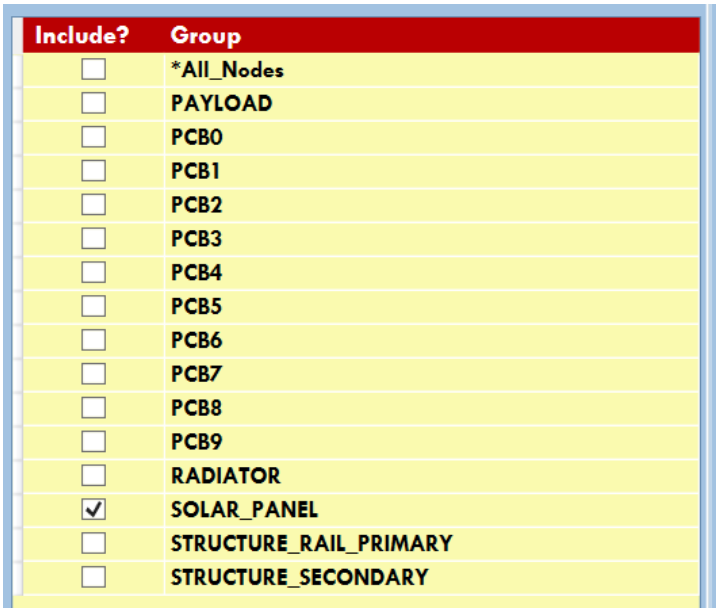
16. *Select to include* the **PCB5.1** node.

17. *Select to include* the **PCB9.1** node.

18. *Select to include* the **RadiatingPower** register.

19. *Select to include* the **SOLAR_PANEL** node group.





Outputs

20. *Select to Include* the “Minimum” and “Maximum” temperature for all nodes and node groups.

21. *Select to Include* the “Maximum” incident heat for the “SOLAR_PANEL” node group.

22. *Select to Include* the “Maximum” value for the “RadiatingPower” register.

Output Requests

Name	Type	Temperature			Incident Heat			Registers		
		Minimum	Mean	Maximum	Minimum	Mean	Maximum	Minimum	Mean	Maximum
SOLAR_PANEL	Group	☑	☐	☑	☐	☐	☑	☐	☐	☐
PCB0.1	Node	☑	☐	☑	☐	☐	☐	☐	☐	☐
PCB5.1	Node	☑	☐	☑	☐	☐	☐	☐	☐	☐
PCB9.1	Node	☑	☐	☑	☐	☐	☐	☐	☐	☐
RadiatingPower	Register	☐	☐	☐	☐	☐	☐	☐	☐	☑

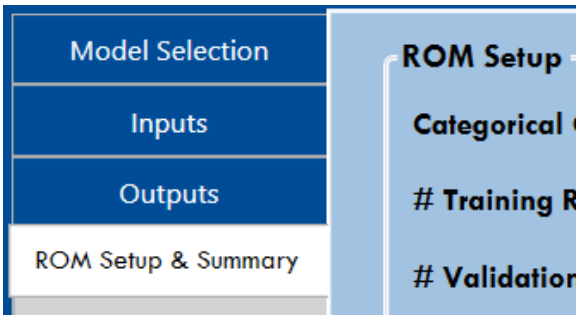
23. *Click* **Check Outputs**.

24. *Click* **OK**.

This step verifies that all outputs are correct. If they are not correct, an information box will pop up with the details on what needs to be changed.

ROM Setup & Summary

Veritrek will automatically move to the *ROM Setup & Summary* tab.



25. *Click* **Yes** to allow *Veritrek* to perform Model Checks.

26. *Click* **OK** to confirm that the model passed the necessary checks.

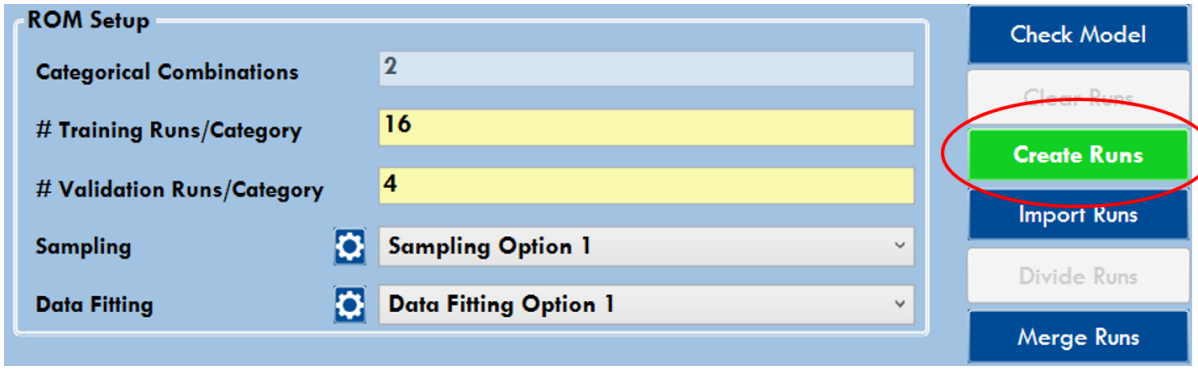
At this point, the *Veritrek Creation Tool* will ask to check model which is required to continue. The *Veritrek Creation Tool* will once again open up and close the selected .dwg file, and notify of a successful model check.

ROM Setup & Summary

27. Leave the # Training Runs/Category at **16**.

28. *Click* **Create Runs**.

29. *Click* **OK** to confirm number of runs created.

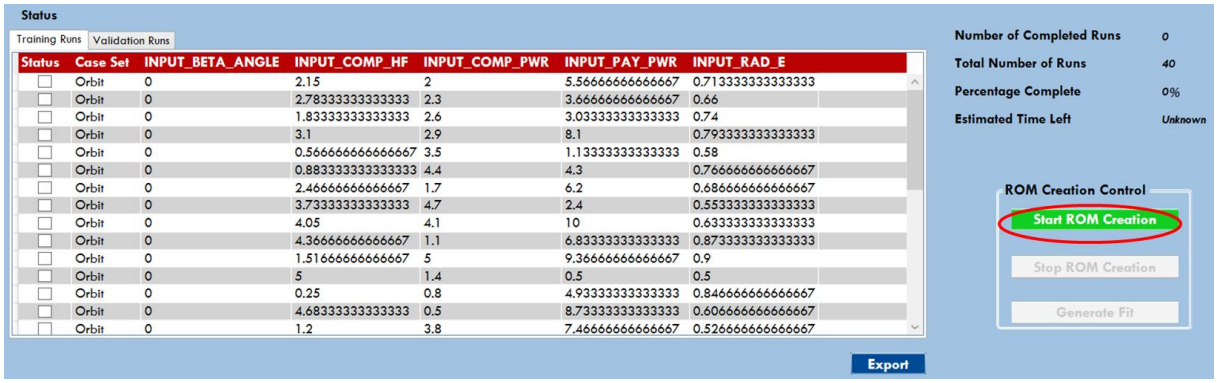


ROM Creation Status

Veritrek will automatically move to the *ROM Creation Status* tab.

30. *Click* **Start ROM Creation**.

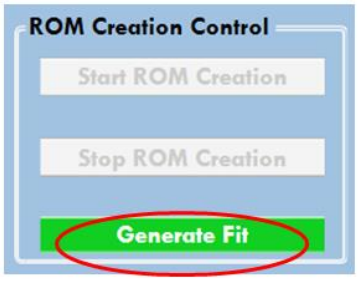
The model will now run for about 1.5 to 3 hours, depending on the speed of the computer performing the calculations. After each run is completed, the *Veritrek Creation Tool* will automatically save the file. If the calculations need to be stopped for any reason, simply click the **Stop ROM Creation** button to stop the current simulation. The **Start ROM Creation** button can then be clicked to resume the calculations. Once complete, proceed to the next step.



ROM Creation Status

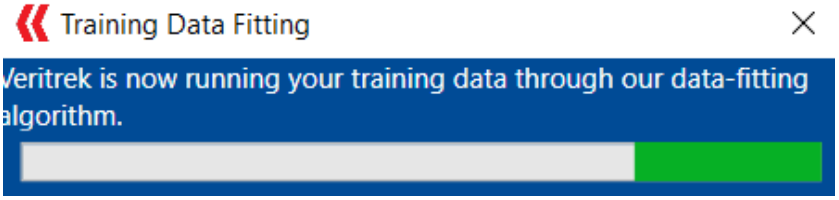
Veritrek will automatically unlock the "Generate Fit" button.

31. *Click* the **Generate Fit** button.



Veritrek will now solve for about 15 minutes. This will create the ROM files.

Once complete, the ROM is fully created. The next steps consist of testing and verifying the accuracy of the ROM.

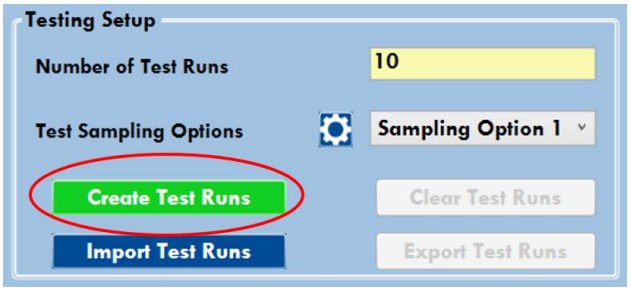


ROM Testing

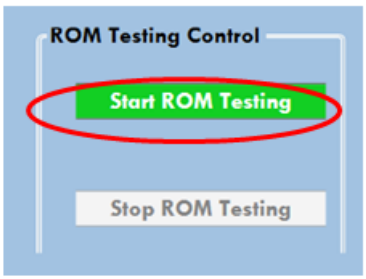
Veritrek will automatically move to the *ROM Testing* tab.

32. Click Create Test Cases.

For this tutorial example, the defaults selected are sufficient for ROM Testing.

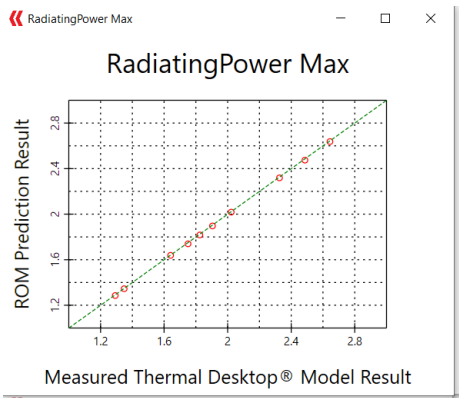


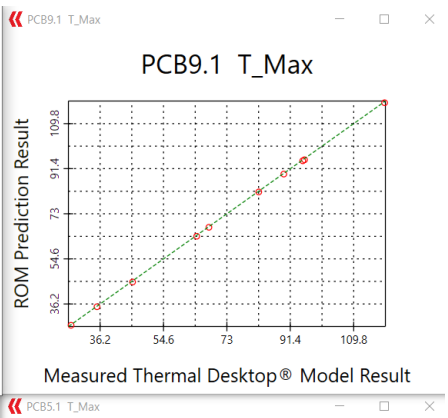
33. Click Start ROM Testing.

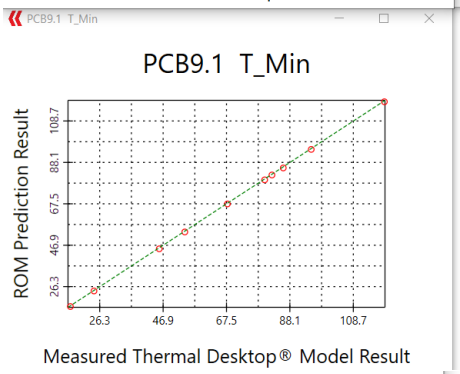


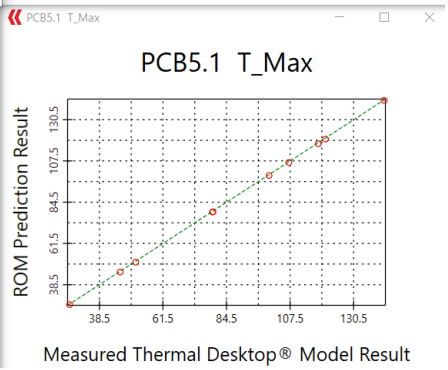
The model will now run for about 20 to 40 minutes, depending on the speed of the computer performing the calculations. After each run is completed, the *Veritrek Creation Tool* will automatically save the file. If the calculations need to be stopped for any reason, simply click the **Stop ROM Creation** button to stop the current simulation. The **Start ROM Creation** button can then be clicked to resume the calculations. Once complete, proceed to the next step.

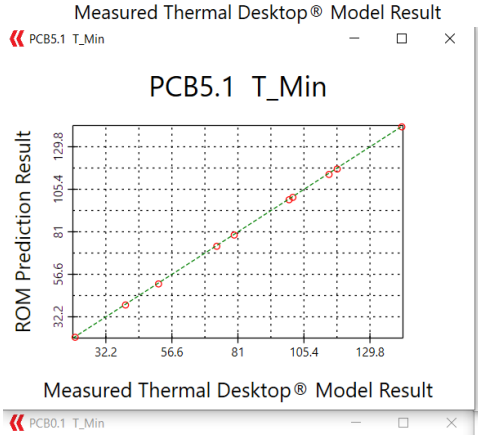
ROM Testing	
34. Click the **Plot Outputs** button for all outputs.	Observe similar results to those shown below.

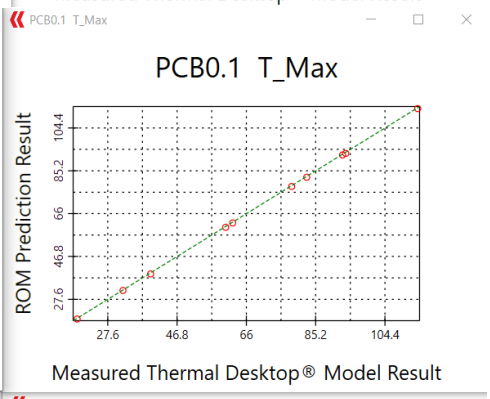


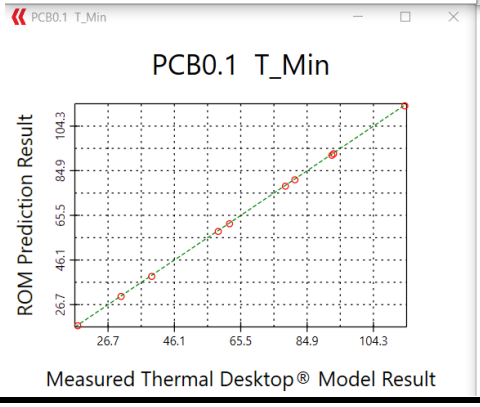


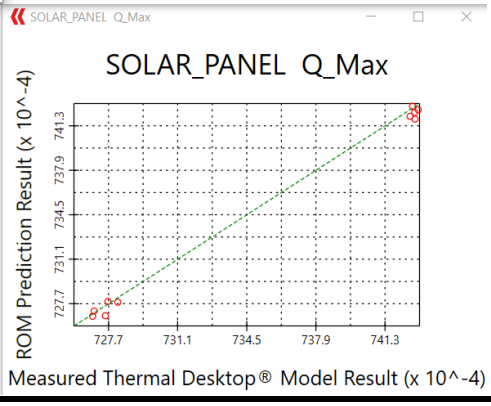




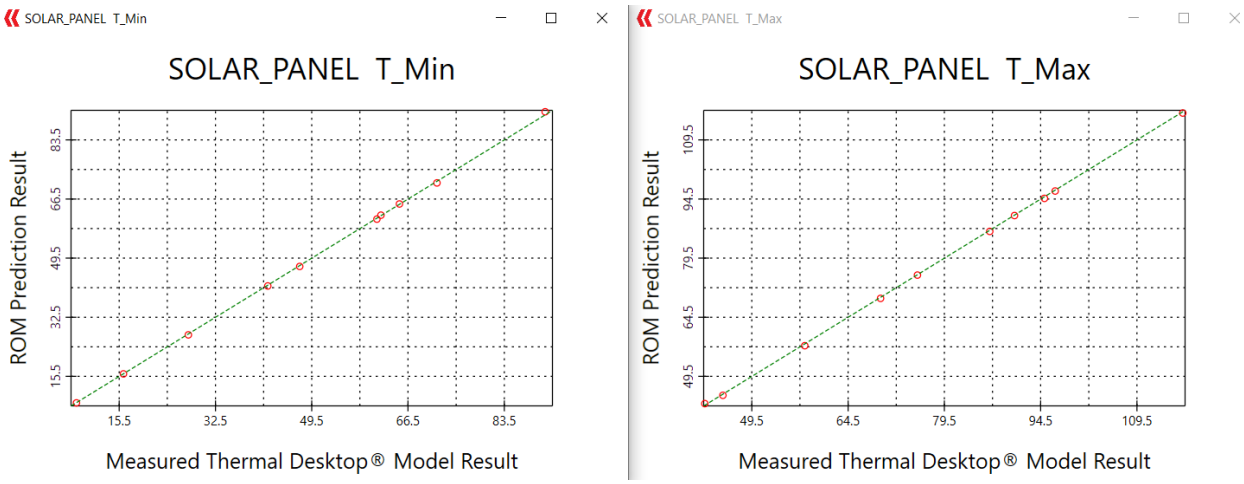








ROM Testing



ROM Summary

35. *Select* the *ROM Summary* tab.

36. Observe similar results to those shown below.

Test Results

Name	Type	Output Type	Mean of Residual	Standard Deviation of Residual
SOLAR_PANEL	Group	Minimum Temperature	-0.293003201308824	0.692576531736624
SOLAR_PANEL	Group	Maximum Temperature	0.168938653707966	0.728836528125103
SOLAR_PANEL	Group	Maximum Incident Heat	-1.57170358203174E-06	2.87467372040289E-05
PCB0.1	Node	Minimum Temperature	-0.0680345523452502	0.0965306366652354
PCB0.1	Node	Maximum Temperature	-0.0664206201848174	0.0953637393448281
PCB5.1	Node	Minimum Temperature	-0.103145256771757	0.112138463038564
PCB5.1	Node	Maximum Temperature	-0.0903422286363821	0.132059559460633
PCB9.1	Node	Minimum Temperature	-0.0620910832248001	0.101114872759994
PCB9.1	Node	Maximum Temperature	-0.049078908703666	0.106175137515978
RadiatingPower	Register	Maximum Value	-0.00115245872872383	0.00228320604547764

4.3 6U CubeSat Demo Example Problem

4.3.1 Description of the VeritrekCT_demoC Thermal Desktop® Model

The easiest way to learn the basics of the *Veritrek Creation Tool* is to create a ROM using the example model provided. The example model is found in the "demo" folder, located in \Program Files\Veritrek\Creation Tool\demo. It is best to copy this folder to another location before performing the demo.

The model, shown in Figure 4-3, is a generic 6U CubeSat. The model includes several isothermal components (such as antennae, batteries, attitude determination and control, propulsion, payloads, radios, avionics, and solar array), along with a deployable radiator. In total this Thermal Desktop® model contains 1795 nodes.

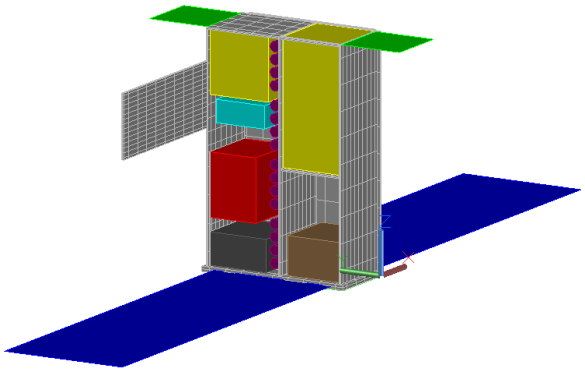


Figure 4-3: VeritrekCT_demoC – 6U CubeSat demo model

A breakdown of the fourteen submodels, and the different Thermal Desktop® objects they include, can be seen in Table 1.

Table 7: Submodels included in VeritrekCT_demoC

Submodel	# of Nodes	# of Conductors	# of Heat Loads	# of Contactors
ANTENNAE	3	0	0	3
ATTITUDE_CONTROL_SYSTEM	1	0	1	4
AVIONICS	1	0	1	4
BATTERY	4	0	4	4
PAYLOAD_1U	1	0	1	5
PAYLOAD_2U	1	0	1	7
PROPULSION	1	0	1	3
RADIATOR_DEPLOYABLE	300	0	0	1
RADIOS	1	0	1	2
SOLAR_ARRAY	2	0	0	2
STRUCTURE_TAB	540	0	0	20
STRUCTURE_TOP_PLATE	200	0	0	6
STRUCTURE_RAIL_SECONDARY	740	0	0	33
TEST	4	3	0	0

The symbol group of “Correlation” will be used in the Tutorial, to explore the ROM parallelization and model correlation capabilities. A list of the symbols in this group, and their descriptions, can be seen in Table 2.

Table 8: Symbols included in VeritrekCT_demoC

Symbol Name	Description
Cond_ACS_to_Structure	Total conductance value between the attitude control system and the CubeSat structure [W/C].
Cond_Avionics_to_Structure	Total conductance value between the avionics stack and the CubeSat structure [W/C].
Cond_Payload1U_to_Structure	Total conductance value between the 1U payload and the CubeSat structure [W/C].
Cond_Payload2U_to_Structure	Total conductance value between the 2U payload and the CubeSat structure [W/C].
Cond_RadiatorHinge	Total conductance value for the deployable radiator hinge [W/C].
PCB_k	Conductivity value of the PCB board components [W/m]C].
SensFac_Abs	Sensitivity factor for the absorptivity value of all components. Added to or subtracted from the nominal value.
SensFac_Emiss	Sensitivity factor for the emissivity value of all components. Added to or subtracted from the nominal value.

In addition to the symbols described above, two case sets are set-up to represent to different TVac test environments. Details can be seen in Table 3.

Table 9: Case Sets included in VeritrekCT_demoC

Case Set	Mounting Flange Temp [C]	Thermal Shroud Temp [C]	Chamber Door Temp [C]
LEO Orbit	n/a	n/a	n/a
TVac Test Hot	35	30	25
TVac Test Cold	-35	-25	0

4.3.2 Preparing the Model for the *Veritrek Creation Tool*

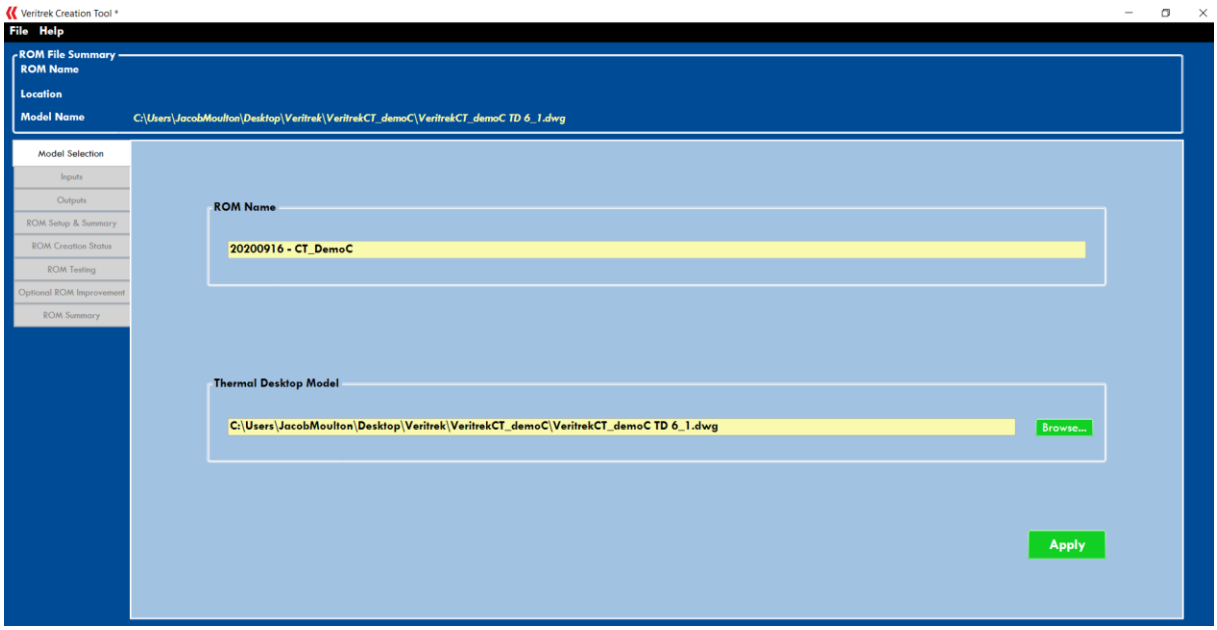
Note: This VeritrekCT_DemoC tutorial takes longer to complete, compared to VeritrekCT_DemoA and VeritrekCT_DemoB.

Copy the model files (VeritrekCT_demoC TD 6_1.dwg, VeritrekCT_demoC.rco, and VeritrekCT_demoC.tdp) from the “demo” directory to another directory and open the model file. Verify that the model is working by running the two case sets.

4.3.3 Click-by-click Solution

<table>
<tr><th colspan="2">Model Selection</th></tr>
<tr><td>Open the tool so that the Main Window is visible.

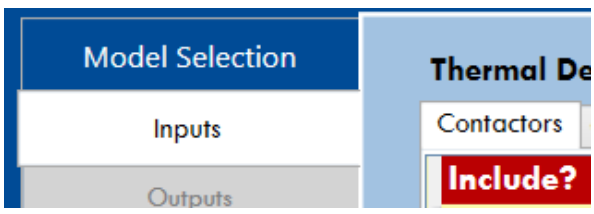
1. Type in “DATE – CT_DemoC” for ROM Name.

2. Select the VeritrekCT_demoC TD 6_1.dwg from its user-specified directory.</td><td>Ensure that the Model Selection tab is selected, and the tool is focused on this tab.</td></tr>
<tr><td colspan="2"> 
</td></tr>
<tr><td>3. Click Apply.

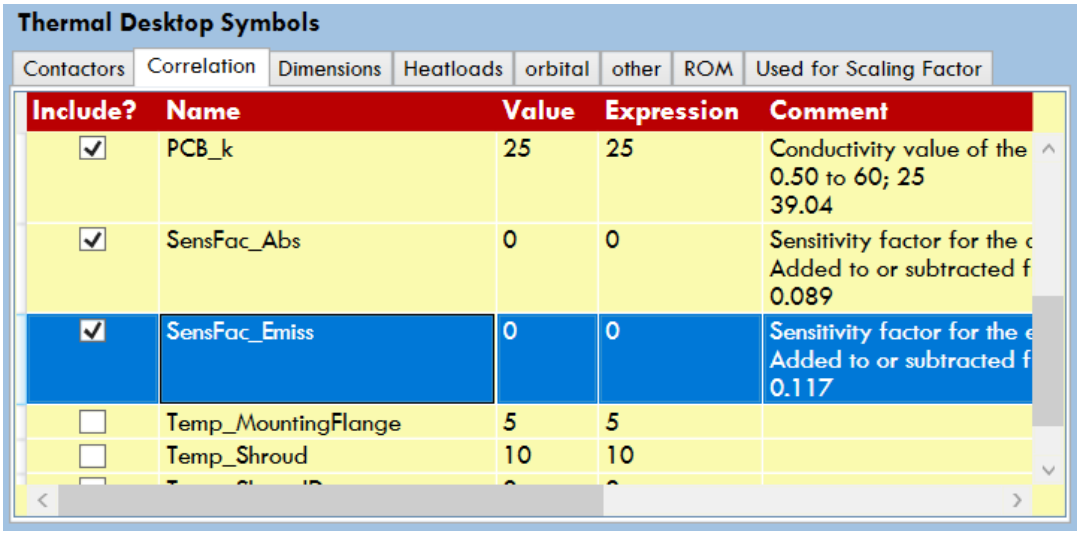
4. Select a location to save the ROM file.

5. Click Save.

Veritrek will automatically move to the Inputs tab.

 
</td><td>At this point, the Veritrek Creation Tool will automatically open the selected .dwg file. After the file successfully opens it will close, and the Inputs and Outputs tabs will become available in the Veritrek Creation Tool.</td></tr>
</table>

Inputs	
6. *Select to include* "Cond_ACS_to_Structure", "Cond_Avionics_to_Structure", "Cond_Payload1U_to_Structure", "Cond_Payload2U_to_Structure", "Cond_RadiatorHinge", "PCB_k", "SensFac_Abs", and "SensFac_Emiss" from the Correlation input factors group.	These checkboxes are in the "Thermal Desktop® Symbols" section of the *Inputs* tab.



7. *Set* the "Minimum Value" for "Cond_ACS_to_Structure" to **0.05**, the "Maximum Value" to **10**, and the "Interpolation Method" to **Continuous**. 8. *Set* the "Minimum Value" for "Cond_Avionics_to_Structure" to **0.05**, the "Maximum Value" to **10**, and the "Interpolation Method" to **Continuous**. 9. *Set* the "Minimum Value" for "Cond_Payload1U_to_Structure" to **0.05**, the "Maximum Value" to **10**, and the "Interpolation Method" to **Continuous**.	

Inputs

10. *Set* the "Minimum Value" for "Cond_Payload2U_to_Structure" to **0.05**, the "Maximum Value" to **10**, and the "Interpolation Method" to **Continuous**.

11. *Set* the "Minimum Value" for "Cond_RadiatorHinge" to **0.05**, the "Maximum Value" to **10**, and the "Interpolation Method" to **Continuous**.

12. *Set* the "Minimum Value" for "PCB_k" to **0.5**, the "Maximum Value" to **60**, and the "Interpolation Method" to **Continuous**.

13. *Set* the "Minimum Value" for "SensFac_Abs" to **-0.07**, the "Maximum Value" to **0.12**, and the "Interpolation Method" to **Continuous**.

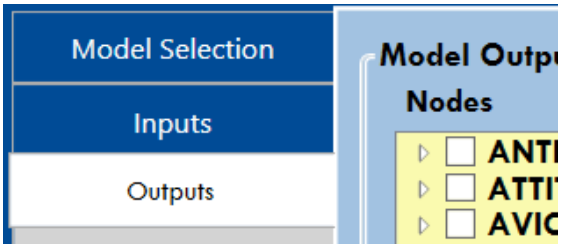
14. *Set* the "Minimum Value" for "SensFac_Emiss" to **-0.01**, the "Maximum Value" to **0.12**, and the "Interpolation Method" to **Continuous**.

Inputs Summary

Group	Name	Nominal Value	Minimum	Maximum	Interpolation Meth
Correlation	Cond_ACS_to_Structure	2.1	0.05	10	Continuous
Correlation	Cond_Avionics_to_Structure	1.1	0.05	10	Continuous
Correlation	Cond_Payload1U_to_Structure	1.1	0.05	10	Continuous
Correlation	Cond_Payload2U_to_Structure	2.1	0.05	10	Continuous
Correlation	Cond_RadiatorHinge	2.5	0.05	10	Continuous
Correlation	PCB_k	25	0.5	60	Continuous
Correlation	SensFac_Abs	0	-0.07	0.12	Continuous
Correlation	SensFac_Emiss	0	-0.01	0.12	Continuous

Navigate to the bottom of the *Inputs* tab, in the Thermal Desktop Case Sets section.

15. *Select* "TVac Test Hot" and "TVac Test Cold" *click* **Add**.

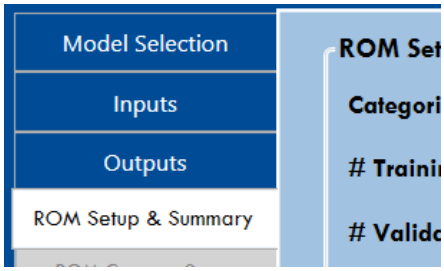
Outputs	
16. *Click* **Check Inputs**. 17. *Click* **OK**. *Veritrek* will automatically move to the *Outputs* tab.  18. *Select to include* the **AVIONICS.1** node. 19. *Select to include* the **BATTERY.3** node. 20. *Select to include* the **PAYLOAD_1U.1** node. 21. *Select to include* the **PAYLOAD_2U.1** node. 22. *Select to include* the **PROPULSION.1** node. 23. *Select to include* the **RADIATOR_DEPLOYABLE.70** node. 24. *Select to include* the **RADIATOR_DEPLOYABLE.72** node. 25. *Select to include* the **SOLAR_ARRAY.2** node. 26. *Select to include* the **STRUCTURE_TAB.35** node. 27. *Select to include* the **STRUCTURE_WALLS.687** node.	This step verifies that all inputs are correct. If they are not correct, an information box will pop up with the details on what needs to be changed.

Outputs	
28. *Select to Include* the "Mean" temperature for all nodes and node groups.	

Output Requests

Name	Type	Temperature Minimum	Temperature Mean	Temperature Maximum
AVIONICS.1	Node	☐	☑	☐
BATTERY.3	Node	☐	☑	☐
PAYLOAD_1U.1	Node	☐	☑	☐
PAYLOAD_2U.1	Node	☐	☑	☐
PROPULSION.1	Node	☐	☑	☐
RADIATOR_DEPLOYABLE.70	Node	☐	☑	☐
RADIATOR_DEPLOYABLE.72	Node	☐	☑	☐
SOLAR_ARRAY.2	Node	☐	☑	☐
STRUCTURE_TAB.35	Node	☐	☑	☐
STRUCTURE_WALLS.687	Node	☐	☑	☐

29. *Click* **Check Outputs**. 30. *Click* **OK**.	This step verifies that all outputs are correct. If they are not correct, an information box will pop up with the details on what needs to be changed.

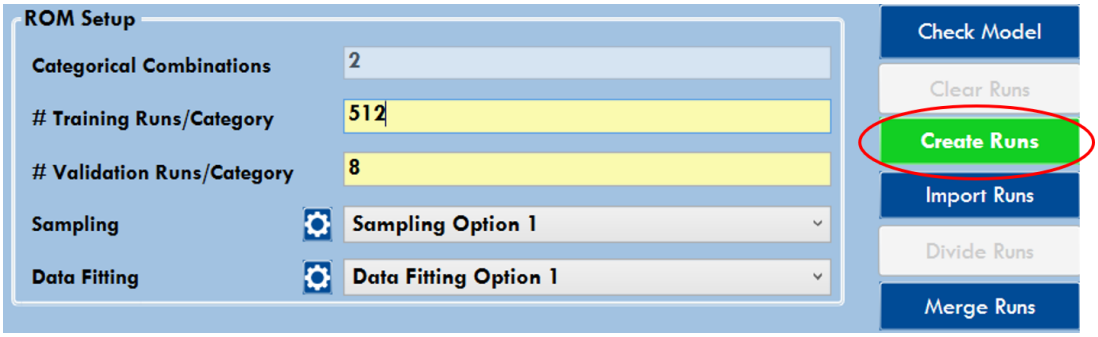
ROM Setup & Summary	
Veritrek will automatically move to the *ROM Setup & Summary* tab.  31. *Click* **Yes** to allow *Veritrek* to perform Model Checks and *Click* **OK** to confirm that the model passed the necessary checks.	At this point, the *Veritrek Creation Tool* will ask to check model which is required to continue. The *Veritrek Creation Tool* will once again open up and close the selected .dwg file, and notify of a successful model check.

32. Set the # Training Runs/Category to **512**.

33. Click **Create Runs**.

34. Click **OK** to confirm number of runs created.

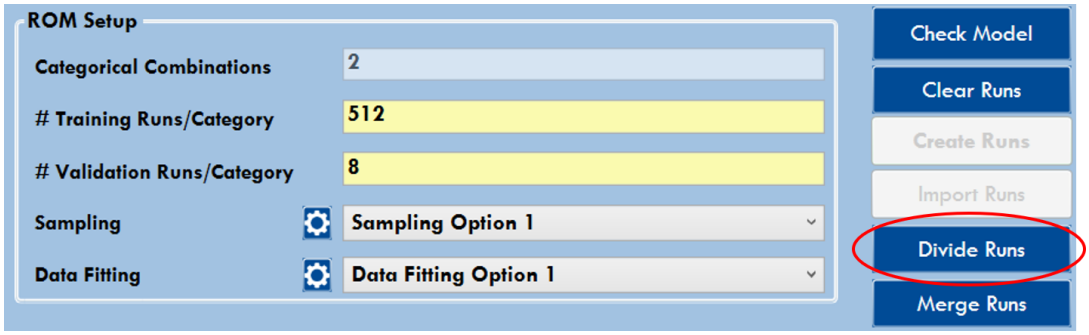
The *Veritrek Creation Tool* will automatically move to the *ROM Creation Status* tab after creating the runs.



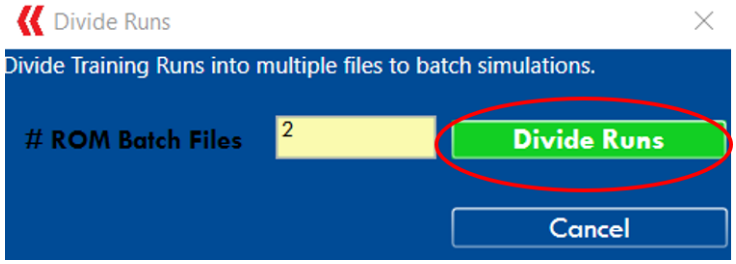
Veritrek will automatically move to the *ROM Creation Status* tab.

35. Navigate back to the *ROM Setup & Summary* tab.

36. *Click* **Divide Runs**.



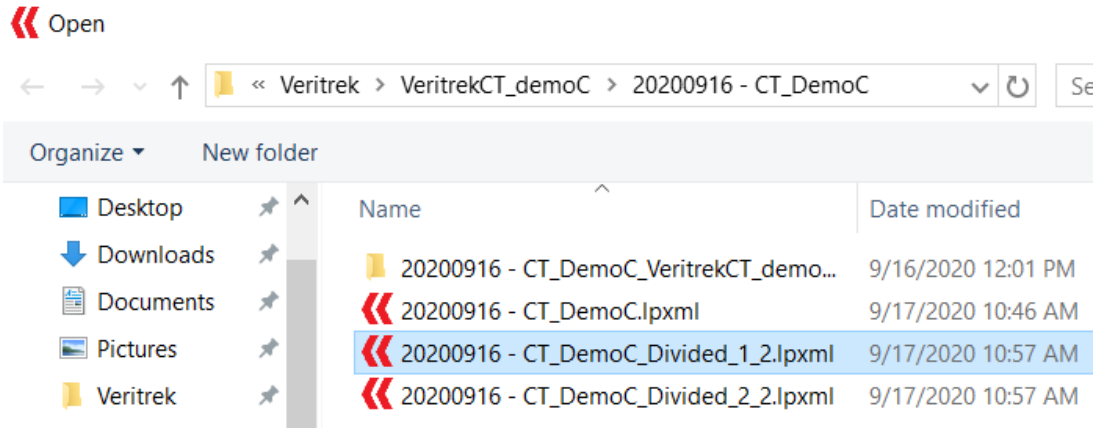
37. Leave the "# ROM Batch Files" at **2** and *click* **Divide Runs**.



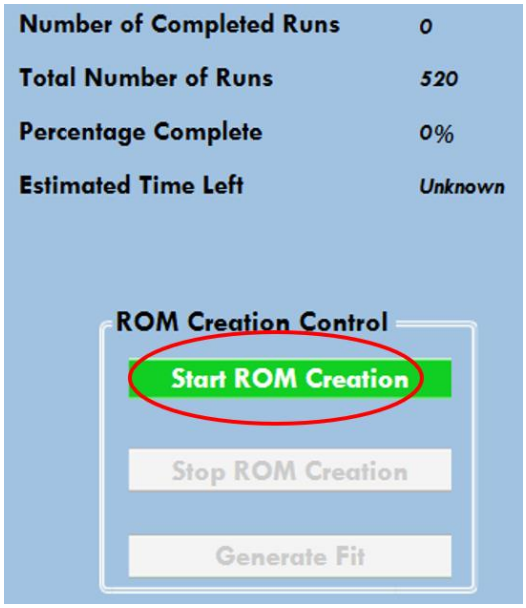
38. *Click* **OK**.

Veritrek will divide the training runs into two separate .lpxml files and provide a pop-up that shows you how many training runs and validation runs were saved in each file, and the name of each file.

39. *Navigate* to File>Open and *Open* one of the two divided .lpxml files.



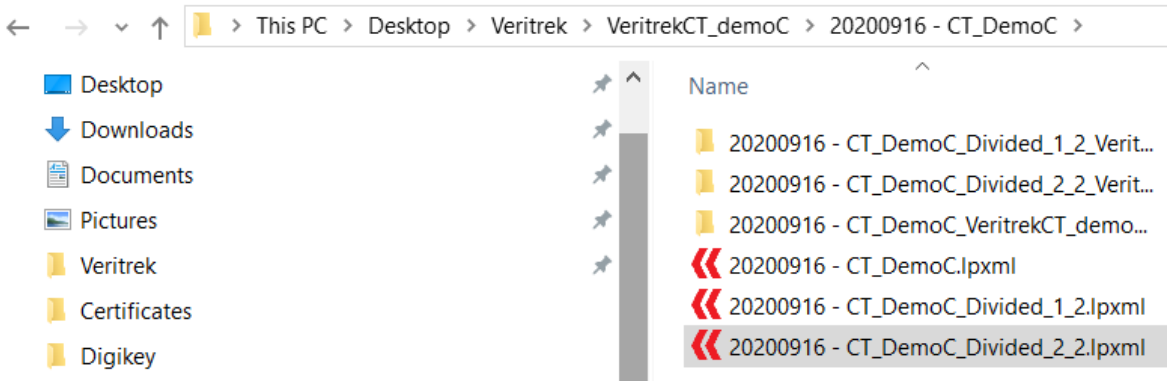
40. *Navigate* to the *ROM Creation Status* tab and *Click* **Start ROM Creation.**



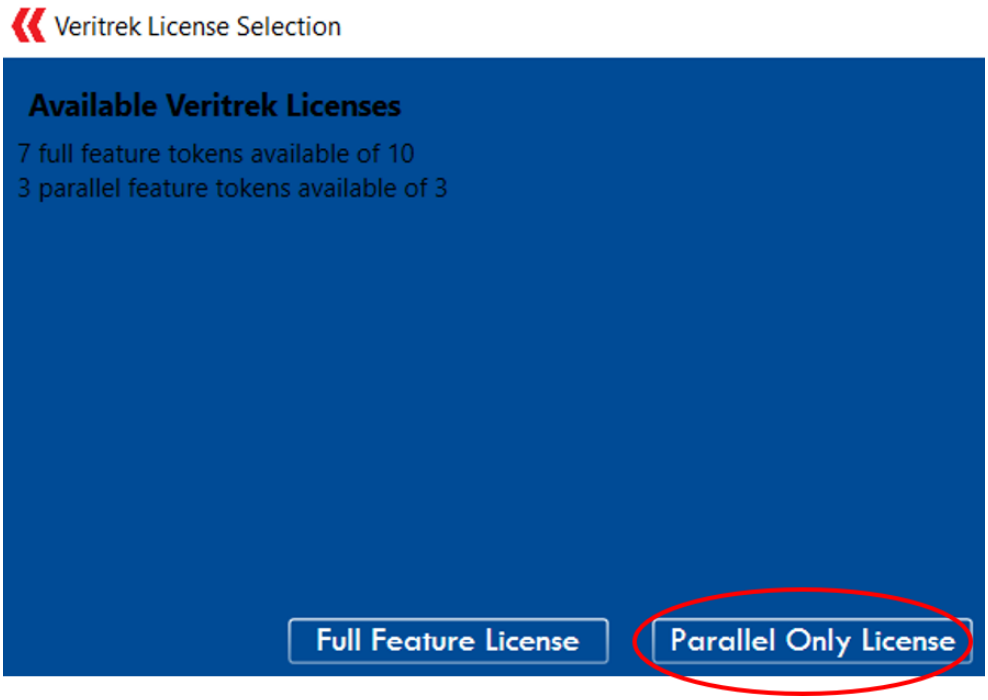
Notice that the Total Number of Runs is half of what it was in the original .lpxml file, as we have evenly split up the training runs into two separate files. We can now run the two .lpxml files in parallel to cut the cost of ROM creation in half.

The model will now run for about 4 to 6 hours, depending on the speed of the computer performing the calculations. After each run is completed, the *Veritrek Creation Tool* will automatically save the file. If the calculations need to be stopped for any reason, simply click the **Stop ROM Creation** button to stop the current simulation. The **Start ROM Creation** button can then be clicked to resume the calculations. Once complete, proceed to the next step.

ROM Parallelization	
41. In your File Explorer, *Navigate* to the second of two divided .lpxml files and *double-click* on it to Open.	Note that this step can be performed on the same machine using a second instance of the *Veritrek Creation Tool*, or the .lpxml file can be transferred to an additional machine to create the training data in parallel. When using a second machine, you will want to copy over the .lpxml file along with the TD model, .rco, .tdp and temporary folder. Upon first opening up the .lpxml file, Veritrek will ask you to point it to the .dwg file.

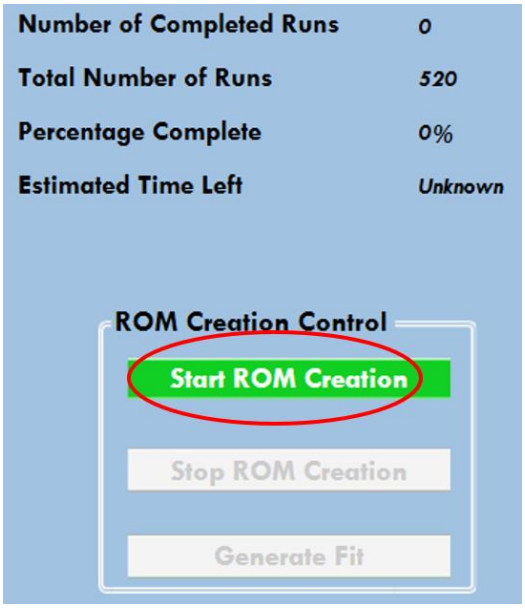


42. *Select* **Parallel Only License** when prompted to select a *Veritrek* license type.

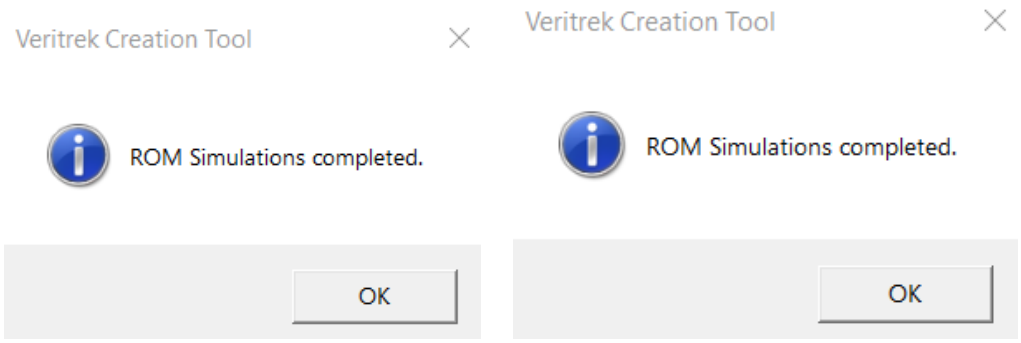


<table>
<tr><th colspan="2">ROM Parallelization</th></tr>
<tr><td>Veritrek will automatically bring you to the ROM Creation Status tab. This is the only tab that can be accessed using the Parallel Only License type.

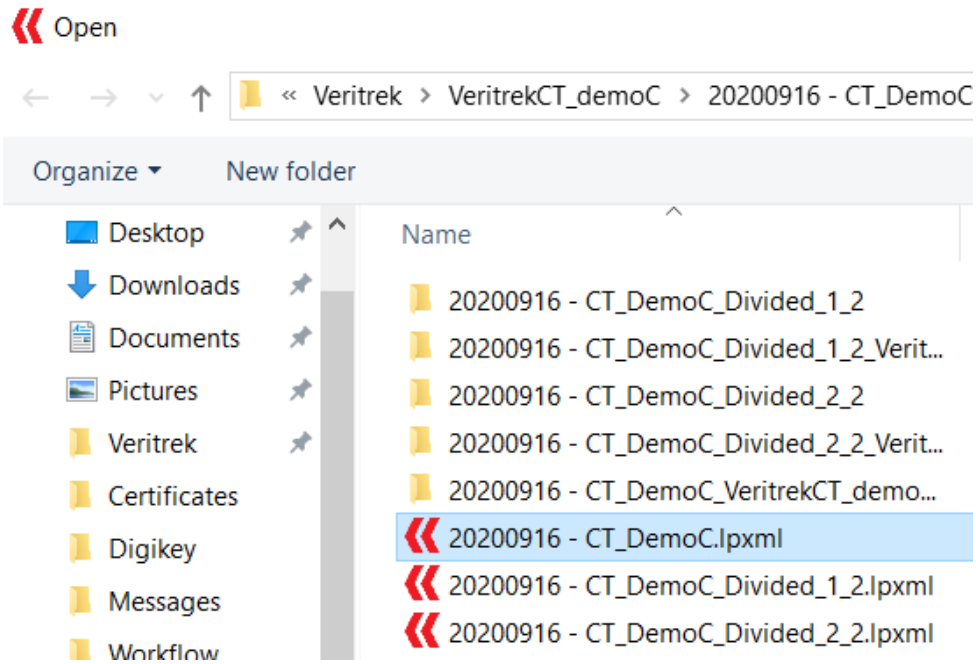
43. Navigate to the ROM Creation Status tab and Click Start ROM Creation.

 
</td><td>Notice that the Total Number of Runs is half of what it was in the original .lpxml file, as we have evenly split up the training runs into two separate files. We can now run the two .lpxml files in parallel to cut the cost of ROM creation in half.

The model will now run for about 4 to 6 hours, depending on the speed of the computer performing the calculations. After each run is completed, the Veritrek Creation Tool will automatically save the file. If the calculations need to be stopped for any reason, simply click the Stop ROM Creation button to stop the current simulation. The Start ROM Creation button can then be clicked to resume the calculations. Once complete, proceed to the next step.</td></tr>
<tr><td colspan="2">Wait until both ROMs have completed generating their training data.

 
</td></tr>
<tr><td>44. Close out of the “Parallel Only License” instance of the Creation Tool.</td><td></td></tr>
</table>

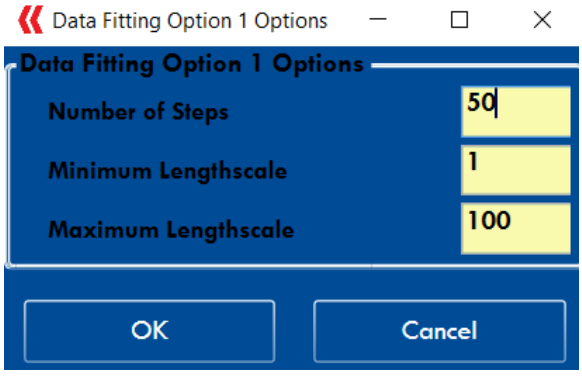
45. *Navigate* to the "Full Feature License" instance of the *Creation Tool*, and go to File>Open to select the original .lpxml file.



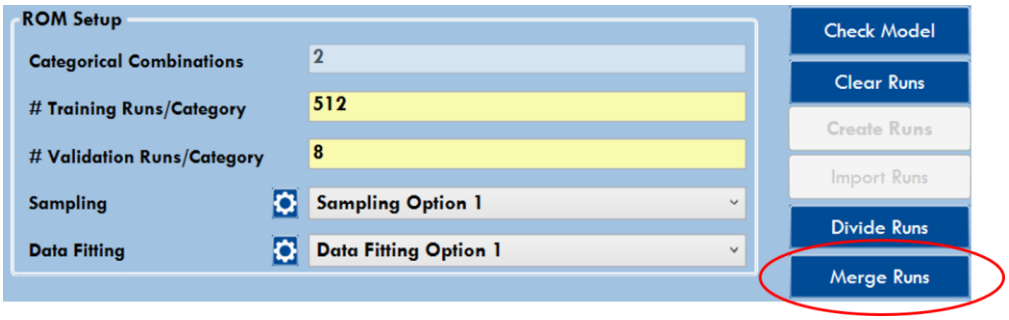
46. *Navigate* to the *ROM Setup & Summary* tab.

47. *Click* the Settings icon for Data Fitting.

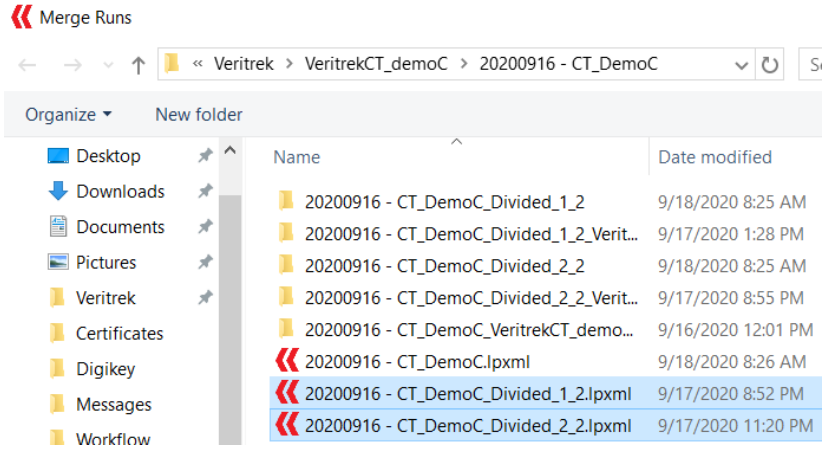
48. *Change* Number of Steps to **50** *and Click* **OK**.



49. Select **Merge Runs**.

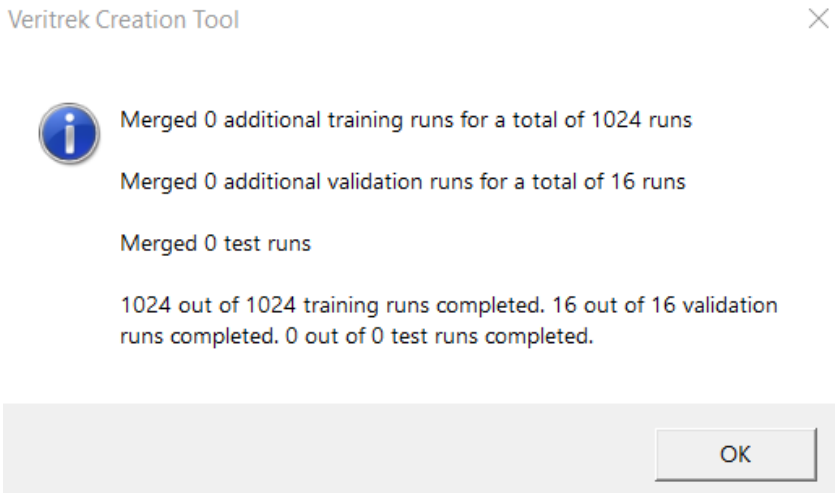


50. *Select* the two divided .lpxmls *and Click* **Open**.



51. *Click* **OK.**

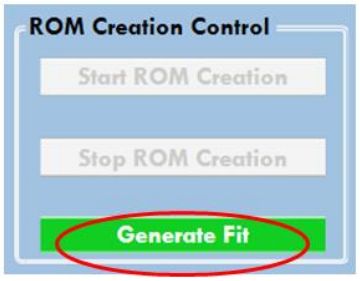
Veritrek will provide a summary of the merged training, validation, and testing runs along with how many of each run have been completed.



ROM Creation Status

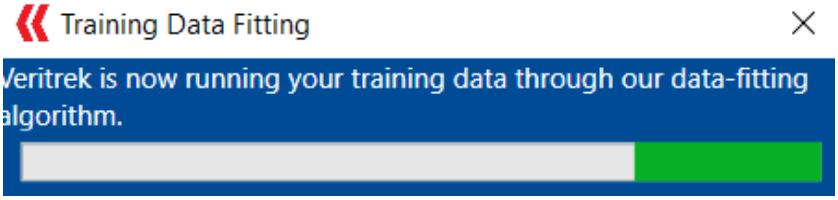
Veritrek will automatically unlock the "Generate Fit" button.

52. *Click* the **Generate Fit** button.



Veritrek will now solve for about 6 to 10 hours. This will create the ROM files.

At this point, the ROM has been fully created. The next steps consist of testing and verifying the accuracy of the ROM.



ROM Testing

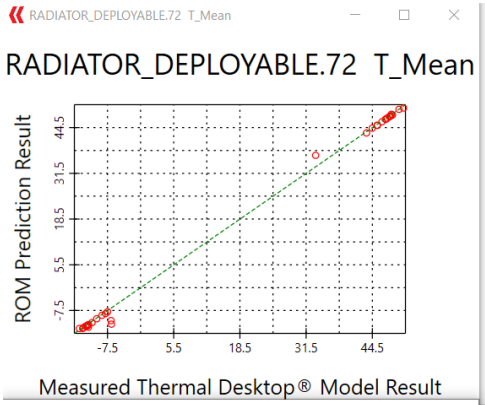
Veritrek will automatically move to the *ROM Testing* tab.

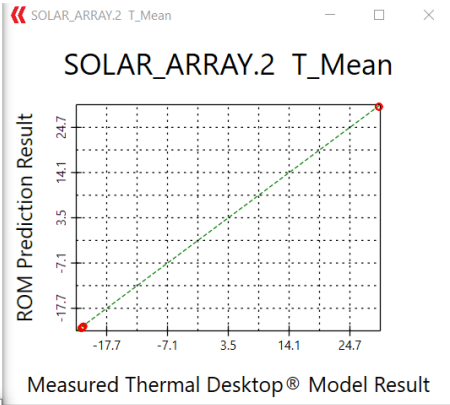
53. *Click* **Create Test Runs**.

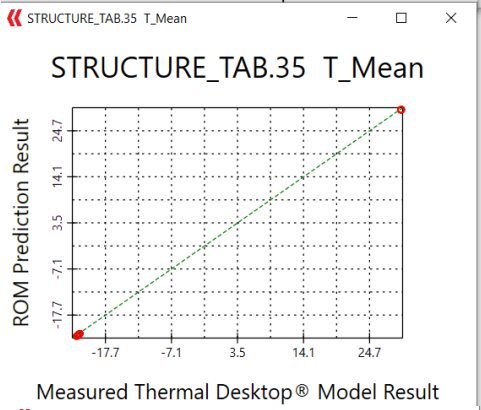
For this tutorial example, the defaults selected are sufficient for ROM Testing.

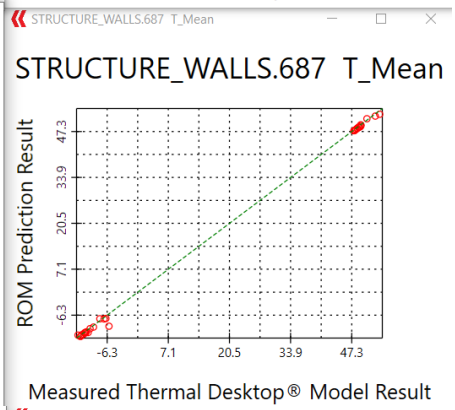
54. *Click* **Start ROM Testing**.

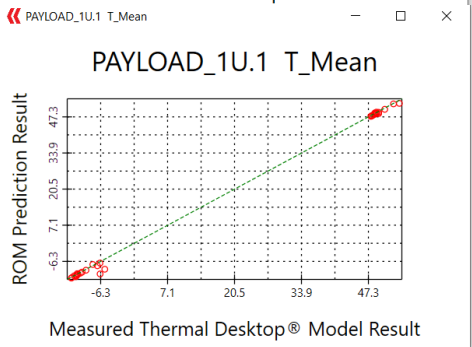
ROM Testing	
55. Click the **Plot Outputs** button for all outputs.	Observe similar results to those shown below.

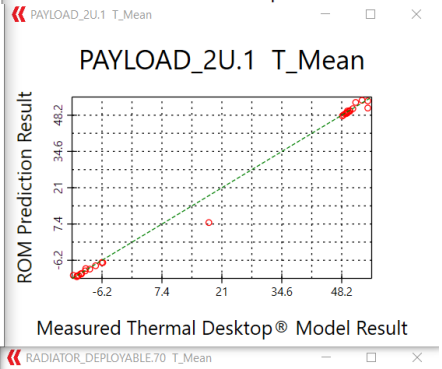


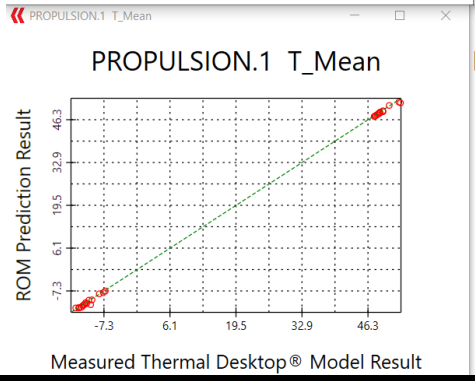


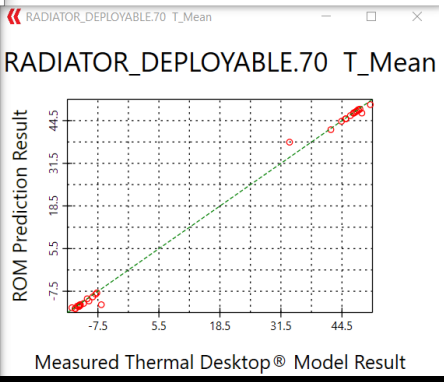




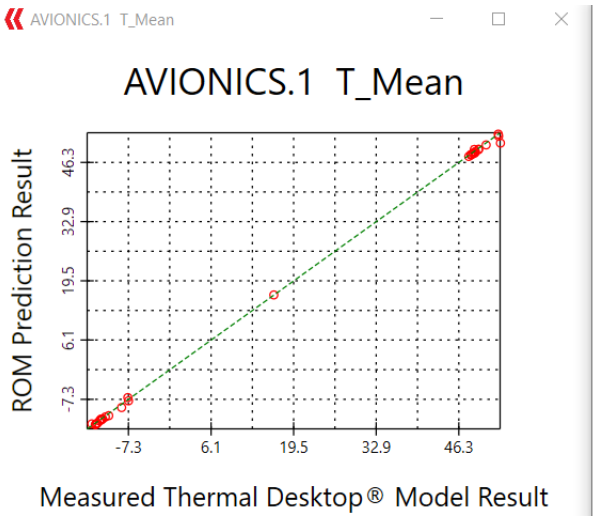


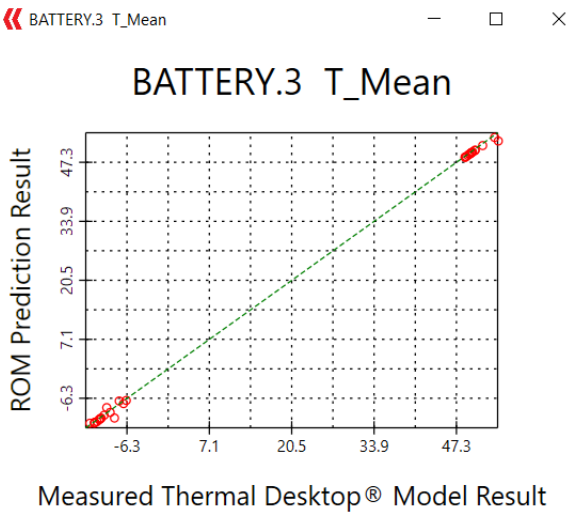






ROM Testing





ROM Summary

56. *Select* the *ROM Summary* tab.

57. Observe similar results to those shown below.

Test Results

Name	Type	Output Type	Mean of Residual	Standard Deviation of Residual
AVIONICS.1	Node	T_Mean	-0.0176897668555389	0.456746624527003
BATTERY.3	Node	T_Mean	-0.0626009617887918	0.593517817769379
PAYLOAD_1U.1	Node	T_Mean	-0.261582987531919	0.982847849233636
PAYLOAD_2U.1	Node	T_Mean	-0.27722617157004	1.86561836613443
PROPULSION.1	Node	T_Mean	-0.0408588339410609	0.372301803875749
RADIATOR_DEPLOYABLE.70	Node	T_Mean	-0.114864041765236	1.24643139204844
RADIATOR_DEPLOYABLE.72	Node	T_Mean	-0.135349745973958	1.16120517978948
SOLAR_ARRAY.2	Node	T_Mean	0.000908789449984404	0.0315733241327374
STRUCTURE_TAB.35	Node	T_Mean	0.0052266123666993	0.0272850656500854
STRUCTURE_WALLS.687	Node	T_Mean	-0.113490557493517	0.666798270746499